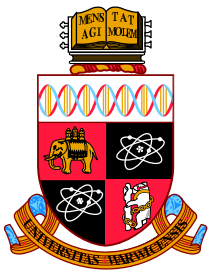
Modelling, Analysis and Control of Multi-Phase Electronically Commutated DC Machines: An Enabling Topology for DC Converter Fed Networks



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Declaration

The work presented in this dissertation was carried out in the Department of Engineering, University of Warwick and at GE Power Conversion Ltd, during the period October 2012 to May 2017 under the supervision of Professor Li Ran and Professor Philip Mawby.

The author wishes to declare that, except for commonly understood and accepted ideas or where reference is made to the work of others, the work in this dissertation is his own. It has not been submitted in part, or in whole, to any other university for a degree, diploma or other qualification. The scale of the routine design and experimental work carried out in support of this thesis was clearly beyond the capability of a single researcher; it is therefore necessary for the author to make the following declaration: The analytical work, modelling, control system formulation & design and implementation on prototype laboratory drives aspects of this research were the work of the author. A large multi-disciplinary team was involved in the design, manufacturing and installation of the laboratory prototype machines and converters. The experimental work and analysis of the results herein are entirely the work of the author.

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Abstract

Multiphase electronically commutated dc machine is a new non-conventional machine and converter topology aimed at dc power generation and delivery systems. This thesis presents a detailed analysis of two multiphase electronically commutated dc machine topologies, firstly, the two level topology then the multilevel topology.

Electronic current commutation processes in these topologies are analysed and electrical machine parameters that influence current commutation and the design of the electronic commutator are exposed. The behaviour of the power electronic commutator circuit is shown to be tightly coupled to that of the electrical machine connected to it and to be inductively dominated during current commutation. Performance, efficiency, footprint and cost are all affected by design considerations arising from the interaction of electronic commutator switching devices and electrical machine. Thus there is an incentive to ensure that the designs of power electronic commutator circuits and electrical machines are matched, allowing the requirements of the system as a whole to be satisfied.

Since these machine and converter topologies depart from the conventional machine and converter topologies, an alternative modelling approach that lends itself well to modelling of the machine and its associated power electronics is presented. The models are used to evaluate the operational attributes of the machine and its associated electronic commutator power electronic circuit and the proposed control schemes.

Results from two prototype laboratory drives built to practically access the viability and fully characterise the operational behavior of these topologies together with the simulation results are presented. Conclusions are drawn concerning the proposed topologies and their associated control strategies.

Nomenclature

Roman Symbols

$\check{L_{mdq}}$ Machine dq magnetising inductance matrix

$\check{L_{mqd}}$ Machine magnetising inductance matrix

B_g Amplitude of fundamental flux harmonic

b_{Sj} Fourier coefficient of stator winding function space harmonics

b_{T_k} Fourier coefficient of stator current time harmonics

$C(s)$ Auxiliary poles signal tracking

D Armature diameter

$F(s)$ Auxiliary poles for disturbance rejection

f_s stator frequency

$F_s(\phi,t)$ Stator mmf waveform

f_{qd_s} Stator dq variables

$G(s)$ Closed loop characteristic equation

I_s Fundamental stator current

$i_s(t)$ Stator current time harmonics

i_{abc_s} Machine stator currents

I_{dc} DC link current

i_{dr} Machine d-axis rotor current

i_{fd} Machine field winding current

I_{gto} GTO current

i_{qr} Machine q-axis rotor current

I_{rms} root mean square current

I_{sc} Short circuit current

I_{wt} Winding phase current

L_c Commutating Inductance

L_{dc} DC Link inductor

L_{end} end winding leakage inductance

L_{kd} Machine rotor d-axis damper resistance

L_{kq} Machine rotor q-axis damper resistance

L_{md} Machine d-axis magnetising inductance

L_{mq} Machine q-axis magnetising inductance

L_{slot} slot leakage inductance

M_n stator phase n mutual inductance

MMF MagnetoMotive Force

mmf magnetomotive force

$N_s(\phi_s)$ Full pitch coil winding function

P_s Park's transformation matrix

P_{dc} dc link power

R_1 Stator phase 1 resistance

r_{fd} Machine field winding resistance

r_{kd} Machine rotor d-axis damper resistance

r_{kq} Machine rotor q-axis damper resistance

$S(\theta)$ Converter switching function

S_{ylv} Sylvester matrix

T_2 Clarke's transformation matrix

t_c current commutation duration

T_e Machine electrical airgap torque

T_m Machine mechanical shaft torque

T_{n+1} Electronic commutator device n+1

U_{swt} electronic commutator switch utilisation

V_c Clamp capacitor voltage

V_h Fundamental harmonic voltage

V_k ripple harmonic voltage

V_s Fundamental stator voltage

v_{abc_s} Machine stator voltages

v_{d_s} Machine d-axis stator voltage

V_{dc} DC link voltage

V_{DMS} maximum surge peak forward and reverse blocking voltage

v_{fd} Machine field winding voltage vector

V_{gto} GTO voltage

v_{md} Machine d-axis magnetising voltage vector

v_{mq} Machine q-axis magnetising voltage vector

V_{pk} peak phase voltage

v_{q_s} Machine q-axis stator voltage

W_f Stator winding factor

y_d Machine rotor network d-axis internal state vector

y_dq Machine rotor network dq-axis internal state vectors

y_q Machine rotor network q-axis internal state vector

FFT Fast Fourier Transform

rms root mean square

THD Total Harmonic Distortion

Greek Symbols

α Electronic commutator firing angle

α_s Stator position offset angle

δ_i electronic commutator balancing current error

γ Parallel electronic commutator circuits connected in series

λ Machine flux linkage

$\Lambda(D)$ Order or degree of the closed loop polynomial equation

$\Lambda(S)$ Order or degree of the polynomial equation

λ_{fd} Machine field winding flux linkage

λ_{kd} Machine d-axis damper flux linkage

λ_{kq} Machine q-axis damper flux linkage

λ_{md} Machine magnetising d-axis flux linkage

λ_{mq} Machine magnetising q-axis flux linkage

μ current commutation interval

ω Controller bandwidth

ω_r Machine rotor angular speed

ϕ_s stator winding function space harmonic phase position

θ_r Machine rotor position

θ_s Stator current time harmonic phase position

ζ Controller damping ratio

Other Symbols

[I] Identity Matrix

[T] Matrix transpose

Acronyms / Abbreviations

A Amps

AC Alternating Current

ac alternating current

COTS Commercially Off The Shelf

CPU Central Processing Unit

CSC Current Source Converter

CSI Current Source Inverter

CSR Current Source Rectifier

DC Direct Current

dc direct current

DQ Direct and Quadrature axis

dq direct and quadrature axis

EMF ElectroMotive Force

emf electromotive force

EMPT Electro Magnetic Transient Programs

F Machine Friction Coefficient

FE Finite Element

FOC Field Oriented Control

FPGA Field Programmable Gate Array

FPSO Floating Production Storage and Offloading Platform

FTI Fast Task Interrupt

GaN Gallium Nitride

GCT Gate Commutated Thyristors

GNA Geometric Neutral Axis

GTO Gate Turn Off Thyristor

HVDC High Voltage Direct Current

Hz Hertz

I Current

IGBT Insulated Gate Bipolar Transistor

IGCT Integrated Gate Commutated Thyristors

J Machine rotor inertia

JFET Junction Field Effect Transistor

kV kilo Volts

LCI Line Commutated Inverter

mH milli Henry

MOSFET Metal Oxide Field Effect Transistors (MOSFET)

ms milliseconds

N Number of machine stator phases

PCB Printed Circuit Board

PIB Power Interface Board

PLECS Piece-wise Linear Electrical Circuit Simulation

PWM Pulse Width Modulation

RB-GCT Reverse Blocking Gate Commutated Thyristors

RBIGBT Reverse Blocking Insulated Gate Bipolar Transistors

RST Polynomial controller

SHE Selective Harmonic Elimination

Si Silicon

SiC Silicon Carbide

V Volts

VBR Voltage Behind Reactance

VSC Voltage Source Converter

VSI Voltage Source Inverter

X Reactance

Chapter 1

Introduction

Direct Current (DC) power generation and delivery systems are becoming an attractive alternative to the well established Alternating Current (AC) power generation and delivery systems. Part of their attraction is due to the fact that dc systems lend themselves well to the integration of alternative electrical energy generation, energy storage and energy delivery systems. One of the fundamental building blocks necessary for flexible dc power generation and delivery systems is the electrical machine and its associated power electronics converter topology. The choice of the electrical machines and their converter topologies employed in such dc systems have a significant impact on the cost, operational performance, protection and reliability of the overall dc system. The research presented in this thesis explores alternative machine and converter topologies that lend themselves well to dc power generation and delivery systems. The proposed machine and converter topologies are aimed at high power applications in excess of 1MW rating.

To fully contextualize the applicability and pertinence of the alternative machine and converter topologies being proposed in this work, its important to firstly give an overview of the existing power generation and delivery systems. In this chapter, a brief review of AC and DC power generation and delivery systems is given to highlight the key merits and shortcomings of these two systems and to also put into context the existing machine and converter topologies currently employed with a view expose key potential benefits that can be derived from the use of alternative machine and converter topologies proposed in this work. Key recent developments

in machine and converter topologies are also briefly highlighted together with some of the challenges currently faced in these recent technologies with the intention of exposing how the proposed machine and converter topologies can either alleviate, circumvent or completely eliminate these challenges.

1.1 AC and DC Power Generation and Delivery Systems

In today's power generation and delivery systems, alternating current systems have become standard in comparison to direct current systems. The invention of the ac transformer was an enabler for ac transmission and delivery systems owing to its key desirable characteristics such as, galvanic isolation, voltage step up/down capability and impedance matching [1]. In recent years significant advances have been made in power electronics technology, both in terms of electrical machines, semiconductor power electronics devices and control hardware architectures [2], [3]. In light of the advances, one can pose the question; can these recent advances in power electronics technology be enablers to dc systems as the ac transformer has been to ac systems? As the demand for flexibility in future power generation and delivery systems increases, power systems that are capable of easily integrating various forms of energy sources such as renewable energy and energy storage systems are desirable and likely to become standard in the future.

In light of these upcoming trends, researchers are beginning to evaluate and seek answers to questions such as; are the reasons that led to the proliferation of ac power generation and delivery systems still valid for some of today's power generation and delivery systems [4], [5], [6], [7] e.g. in aviation, automotive, marine, offshore and renewable energy sectors? From time to time, there is a need to review the current technologies with a view to identify potential areas that need further research and development to ensure that the best technology is adopted for future power generation and delivery systems. The advantages of ac in power generation and delivery systems are well documented in literature and will not be repeated here [8]. In these systems, power is generated, transmitted and distributed at fixed frequency, 50 Hz and 60 Hz ac

systems have been adopted internationally as standard. However, investigations in DC systems have highlighted some beneficial characteristics in comparison to ac systems that can be exploited to give a superior system with respect to system design, build, maintenance and operational requirements for certain power generation and delivery systems [9],[10].

1.2 DC Systems

Research has shown that for a given cross section of power cable and a given insulation strength, circa 10 percent more power can be transmitted using dc systems [11],[12]. This figure improves as cable length increases [13],[14]. It has also been long established that ac systems require additional reactive power compensation to accommodate charging current of the ac cables [12]. Additionally, harmonics, power factor, synchronisation, switching transients and fault currents are all rendered less problematic in dc systems and thus result in a simplified systems [15]. Furthermore, as demonstrated by HVDC links, the advantages of DC transmission systems as step out length increases are well documented in academia and in manufacturer's publications [16], [17]. By their very nature, DC systems lend themselves well to the integration of alternative energy sources as in most, if not all cases the power is generated at variable frequencies and requires ac/dc conversion stages before its converted back to ac for grid integration.

1.3 Potential DC Systems Application Areas

However, in some applications that are decoupled from the ac grid, there is no need for the dc/ac conversion stages for transmission/distribution as the power can be distributed to the various loads as dc power. For example in marine power system applications such as, Floating Production Storage and Offloading (FPSOs) platforms for oil and gas industry, offshore wind and tidal renewable energy generation and collection stations, ship power and propulsion systems as shown in figure 1.1, etc, there is no requirement for generating and distributing the power at fixed 50/60 Hz frequencies any more as the power generation and delivery systems in these applications are not directly tied to the

ac grid[18]. As such, the type of power generation electrical machine technology used, machine frequency, number of phases, topology, choice of power delivery architecture e.t.c. become free parameters that offer extra degrees of freedom in the system design. These parameters can be exploited to design optimised power generation and delivery systems for these applications.

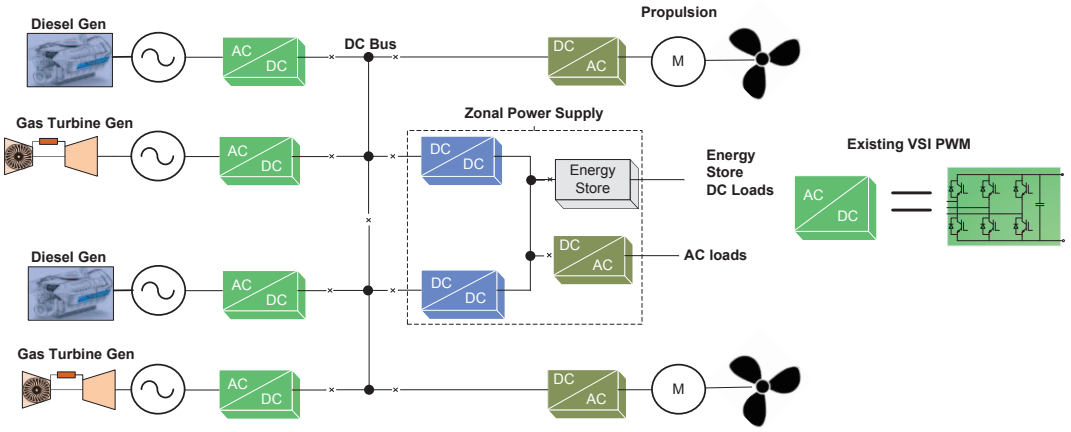

Fig. 1.1 DC Based Marine Power System

1.4 DC Systems Challenges

One of the key known drawbacks that have prohibited the uptake of dc systems is the protection circuit breakers for dc systems[17],[18],[19], [20],[5]. It's well known that ac circuit breakers benefit from zero volts/amps crossings of the ac waveforms that give improved likelihood of extinguishing the fault current arc when the circuit breaker operates. On the contrary, in dc systems there is no zero crossings and fault current interruption has been a challenge [21, 22] and suitably rated switchgear tend to be bulky and expensive in comparison to ac switchgear. However, it must be borne in mind that in present and future dc systems, all of the generated power passes through some form of power electronic conversion input/output stage before it gets transmitted, distributed and delivered to the various loads. With the rapid advances in power electronics research in recent years, power electronic converters with fault current limiting capabilities are becoming standard [23],[24]. It's therefore conceivable, subject to further research, for dc power generation and delivery systems

with embedded power electronic converters to be designed to circumvent or mitigate the current limitations of dc circuit breakers in dc generation and delivery systems.

Some recent studies have focused on alternative means of fault current interruption and suppression using superconductors that rapidly quench and revert to high resistive state to reduce the prospective fault current magnitude[25]. However, the reliability, cost and commercial availability of cryogenic equipment are some of the major drawbacks of this solution. Several studies in solid state circuit breakers capable of interrupting fault currents within 20 ms have also been reported [19]. All these approaches include the addition of extra equipment in the dc system to interrupt the full fault current. An attractive alternative approach would be to actively control the power electronic conversion stages of the dc system to rapidly limit (starve) the energy transfer to the faulty section of the system upon fault detection. Research into such smart protection schemes for dc systems will remove the high duty requirement for dc circuit breakers to interrupt the full prospective system fault current, thereby allowing smaller, low duty and low cost dc circuit breakers to be used merely as offload isolators. However, not all power electronic machine and converter topologies lend themselves well to this fault current limitation protection strategy in dc systems.

The proposed machine and converter topologies do facilitate fault current limitation and protection when applied to dc systems. The machine and converter topologies considered in this work are capable of producing fixed and variable dc voltage outputs when employed on power generating systems subject to whether the prime-mover employed runs at fixed speed or variable speed.

For variable speed prime-movers such as wind turbine alternators and motoring applications, the topologies considered in this work output variable dc link voltages and as such will require dc/dc converters for connection to fixed dc bus voltages of the power delivery system as highlighted in [26]. Figure 1.2 shows an example of a dc/dc converter that can be employed for interfacing the variable dc output of this topology to a fixed dc bus voltage of the dc power delivery system. In this topology device T1, T2 & T5 are actively controlled for positive machine output dc voltages, T1 & T2 are controlled to generate active voltage vectors and T5 is controlled to generate zero voltage vector to freewheel the machine output current. Similarly for negative output machine dc link voltage, device T3, T4 are actively controlled to

generate active voltage vectors with device T5 controlled to generate zero voltage vector to freewheel the machine output current. This is juts one example of many dc/dc converter topologies that can be employed with proposed machine topology. With such dc/dc converters, full four quadrant operation can be achieved for motoring applications.

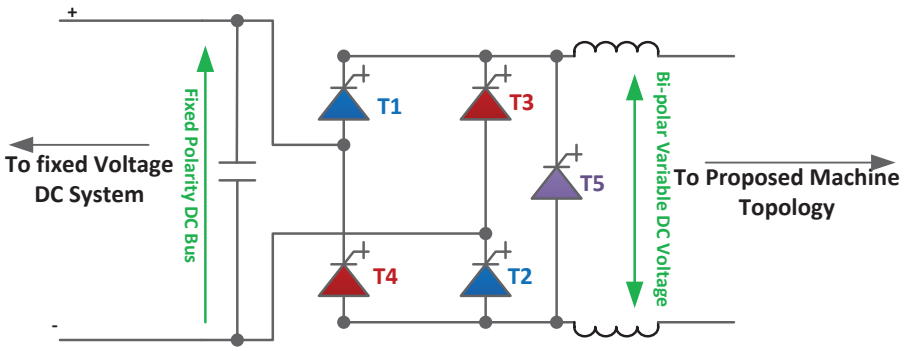

Fig. 1.2 DC/DC Converter Topology for Interfacing to Fixed DC Systems

1.5 Electrical Machines

Electrical machines can be classified into two main categories, asynchronous and synchronous machines. With asynchronous machines, the asynchronous nature of operation comes from the slip (speed difference required for torque production) between the rotational speed of the stator field and that of the rotor field. On the other hand synchronous machines have special rotor construction that enables rotor field to rotate at the same speed i.e. in synchronization — with the stator field. Single fed (squirrel cage type) and doubly fed induction machines fall into the asynchronous machine category and feature machine excitation via the machine stator winding. Single fed asynchronous machines require converters rated to deliver rated torque and are widely used in industry [27]. Doubly fed asynchronous machines are rarely used nowadays with the exception of wind applications where Doubly Fed Induction Generators (DFIGs) are still used. DFIGs require smaller converter kVA rating which depends on the required machine speed control range. Owing to direct grid connection

of the machine stator and a fractionally rated converter, DFIGs have inherent poor grid fault ride through capability [28].

Switched reluctance, synchronous reluctance, permanent magnet, wound rotor synchronous machines fall into the synchronous machine category and all rely on separate rotor excitation. Switched reluctance machines have inherent disadvantages of high torque ripple, acoustic noise, vibration and low overload capability[29]. Synchronous reluctance machines suffer from torque ripple and poor power factor [30],[31]. For these reasons, both switched and synchronous reluctance machines will not be considered in this work. Wound rotor synchronous machines are in wide use today for high power generation and motoring applications [32],[28]. Permanent magnet synchronous machines are gaining attention in low speed direct drive wind generators [33],[34]. However, the main drawbacks of permanent magnet machines are the presence of cogging torque, the cost of permanent magnets and also the risk of permanent demagnetisation of the rotor magnets under fault conditions.

For purposes of highlighting the machines being considered in this work, the electrical machines have been grouped into two further categories depending on whether mechanical means of current commutation is employed or not, as depicted in figure 1.3. Brushed electrical machines include DC, wound field synchronous and wound rotor induction machines [35]. Brushless machines include squirrel cage induction, permanent magnet and reluctance machines which do not require mechanical means of current commutation [36]. The machine topologies proposed in this work are derivatives of the synchronous machine category highlighted in bold red in figure 1.3 and aim to address the key drawbacks of brushed electrical machines for high power applications by employing electronic means of current commutation as well as utilising multi-phase stator phase windings. Permanent magnet means of excitation is also applicable to this machine and converter topology.

1.5.1 Multiphase Electrical Machines

Conventional three phase machines are standard in industry and power generation units mainly driven by the need to connect to the grid power supply. However, in applications such as dc power systems where the generating units are decoupled from

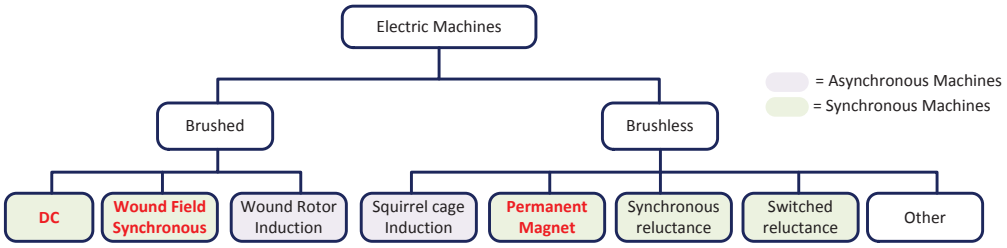

Fig. 1.3 Electrical Machine Categories

the grid, there is no requirement for adhering to the standard three phase machine topology as highlighted earlier. Increasing the machine phase number beyond three can yield significant benefits such as; (a) increased machine and converter fault tolerance, (b) reduced per phase VA rating for a given machine power, (c) reduced torque ripple and machine noise and vibration signature, (d) improved torque density by harmonic injection, (e) increased efficiency owing to the reduced lower order space harmonics [37], [38]. By increasing the machine phase number beyond three, machine active material utilisation factor is increased and machine harmonic performance is enhanced by the consequential decrease in detrimental low order space and time harmonics that give rise to undesirable torque pulsations and mechanical resonance issues [39], [40],[41], [42]. When stator phase number increases, the unwanted harmonics are pushed to higher orders where their amplitudes diminish in inverse proportion to their order. The capacity of a machine can be expressed as $S = N.V.I$, where N= number of phases, V & I are phase voltages and currents. It therefore follows that for a given machine rating, increasing the number of phases N, reduces the phase VA rating. Consequently, the paralleling and seriesing of power electronic devices to achieve higher phase VA ratings can be avoided, thereby eliminating problems associated with static and dynamic voltage and current sharing of the power electronics devices. Recent comprehensive reviews of multiphase machines are given in [43],[37]

Recently, there has been an upsurge of interest in multiphase machines for applications such as electric ship propulsion, hybrid electric vehicles and aircraft generating systems [44], [45], [46], [47] to exploit these desirable characteristics. However, most of these converters are based on VSC/VSI power electronic topologies and suffer the afore mentioned fault current limitation issues when applied to dc power generation

and delivery systems. This research seeks to explore the use of current source based multiphase machine topologies for dc power generation and delivery.

For dc power generation and delivery systems to be fully accepted as an alternative to ac power generation and delivery, research efforts on this subject have to go beyond the generators and power electronics topologies. They must also address the knowledge gap and challenges in system level integration issues in dc systems. This knowledge gap is evidenced by the current lack of international standards on dc generation and delivery systems. Research on system architecture design and optimisation, energy flow control and system level modelling for such distributed systems with a large penetration of multiple power electronic converters is imperative. For example, the ability to assess the impact of issues such as; system response to dynamics caused by interactions between the power electronic converters (subsystems), system response to changes in power demand, system behaviour during non-linear events such as switching, load rejections, fault conditions and impact of negative incremental impedance characteristic of certain loads on the dc delivery system is paramount [48],[49].

A number of approaches to address these system level challenges have been published in [50] and others. Recent studies have shown that system level modelling and simulation provides a convenient means of studying the behaviour of these systems in great detail [51], [52]. A variety of methods have been reported in literature including detailed device level models of power electronic systems, small signal average models, large signal average models, generalised average models, exact models just to name a few [53],[48], [54],[55], [56]. Most of these can be implemented in continuous and discrete time formulations and other in frequency domain. Each of these modelling approaches has its own characteristic advantages and drawbacks depending on its intended purpose as summarised in [57]. For example, transient simulations using detailed switch models of power electronic systems will represent the converter PWM switching harmonics but such simulations require significant computer resources and long simulation times. When many power electronic converters are used in power systems, this simulation approach becomes impractical. On the other hand, small signal modelling techniques are useful in designing closed loop control schemes for power electronic converters. However, they do not lend themselves well to the full behavioural characterisation of a system for example during large system

disturbances. The limitation comes from the fact that these models are linearized around the quiescent operating point and are valid for small disturbances around that operating point. Large signal average models do not model PWM switching harmonics, but are suitable for determining the system's response to large dynamic changes in the power system (e.g. large load changes). With large signal modelling, the dynamics resulting from control system and power system interactions can be revealed [58]. To facilitate full characterisation of the new proposed dc power generation and delivery topologies, further research is required to develop generic large signal time domain models and small signal frequency domain simulation models to facilitate full characterisation of these new dc power generation and delivery architectures.

This research work will aim to address some of the key challenges highlighted in this chapter to enable the design and characterisation of dc power generation and delivery systems with multiphase electronically commutated DC machines. This will include proposals and analysis of two level and multilevel current source type electrical machine and power electronic topologies, modelling and simulation and technology demonstration to validate the proposed topology.

1.6 Research Objectives and Contributions

This research considers alternative novel electrical machine and converter topologies for use in dc systems for either mechanical to electrical power conversion (generating applications) or electrical to mechanical power conversions (motoring applications). The main research objectives are:

- To explore new electrical machine and power electronic converters supplied from dc systems to address some of the challenges faced with the existing electrical machine and converter topologies.
- To develop simulation models of these machine and converter topologies to facilitate full characterisation of the operational behavior, merits and drawbacks of these topologies.
- To formulate suitable control strategies for these novel machine and converter topologies.

- To experimentally validate the proposed machine and converter simulation models.
- To experimentally validate the proposed electrical machine/converter topologies, the associated control strategies and performance evaluation and topology efficiency characterisation.

The thesis makes the following original contributions to the wider research in the area of dc power systems:

- Introduces new multiphase/multileve electrical machine and converter topologies applicable to dc systems.
- Characterises the operational behaviour of these new topologies and evaluates the key performance characteristics, advantages and disadvantages of these topologies.
- Introduces suitable methods of modeling these new electrical machine and converter topologies and the benefits.
- Introduces and validates new control strategies for these machines and the associated power electronic converters topologies.
- Introduces mechanical integration of power electronics converter topologies in the machine stator housing to yield compact drive footprint.

1.7 Thesis Outline

Chapter 1

This introduction chapter gives a literature review and outlines the key motivation for this work.

Chapter 2

Introduces multiphase machine concepts applicable to two level multiphase electrical machine topology and multilevel electrical machine topologies. It outlines the operating principles of these two topologies. Electronic machine current commutation of the

machine converter topology is described and compared to that of classical dc machines with mechanical commutators.

Chapter 3

This chapter focuses on the two level multiphase electrical machine topology and its associated power electronic converter topology. It outlines the operating principles of this two level topology. Electronic machine current commutation for this topology is described. Two level multiphase electrical machine topologies with even and odd number of phases are discussed and a comparison of their merits and drawbacks is given.

Chapter 4

This chapter extends the multiphase machine concept to multilevel machine and power electronic converter topologies. These topologies are investigated and their operational characteristics and desirable attributes are highlighted.

Chapter 5

A review of modeling techniques applicable to the machine/converter topologies outlined in chapters 1 & 2 is given. Suitable modeling approach is given, the mathematical model derivation and implementation is described. This method enables characterisation and detailed design of the power electronic converter and verification of the proposed control schemes.

Chapter 6

This chapter details the derivation and implementation of the controller used for most of the control loops in chapter 7. The control architecture is based on an elegant pole placement method that uses polynomial solution of the Diophantine equation. Equations for the discrete z-domain and continuous s-domain designs of the controller are derived. Advantages of such a controller are highlighted and methods of tuning the controllers are given.

Chapter 7

Suitable control schemes for the proposed electrical machine and converter topologies are given. The design of the control loops are described and the equations governing their behaviour given.

Chapter 8

Two of the novel electrical machine and converter topologies are experimentally validated. The design of a comprehensive experimental test rig capable of allowing both motoring and generating applications to be validated is presented. This considers the power electronics design implementation and control design implementation.

Chapter 9

Comparison of measured and simulated results is given in this chapter. A number of operational scenarios are presented to validate the simulated behaviour of the proposed machine and converter topologies for both even and odd number of stator phases.

Chapter 10

A final consideration is given that puts the technical achievements of the presented work in a wider context and highlights areas for further research.

Chapter 2

Machine and Converter Topologies

2.1 Introduction

Having alluded to the benefits of multiphase electrical machines highlighted in the previous chapter, it is imperative to further explore machine topologies that fully exploit these benefits. Classical brush commutated dc machines offer some of these benefits and are capable of producing high air gap shear stress. However, their practical torque density performance is limited by the mechanical brush commutation process. A closer look at the armature windings of classical dc machines reveal that they are in fact mechanically commutated multiphase machines with a large number of armature phases, five to seventeen and even higher. If the undesirable limitations of the mechanical brush commutator can be eliminated, a multiphase dc machine topology becomes an attractive proposition. Owing to recent advances in power semiconductor device technology and control hardware, it is possible to completely eliminate the mechanical brush commutator and replace it by electronic means of armature current commutation.

In this chapter, novel electronically commutated multiphase dc machine topologies and their associated power electronic converter configurations are discussed. The operating principles of each of these topologies will be outlined and the benefits and drawbacks will be highlighted. The major motivation of this work is to advance knowledge on these new alternative machine and converter topologies that potentially lead to increased efficiency, reduced footprint and overall cost of the drive system,

i.e. machine and converter. Integration of the converter power electronics within the machine housing will significantly reduce the overall drive footprint. As such, the topologies explored in this work are intended to facilitate this machine and converter integration. One of the contributing factors to the efficiency of the drive system is the converter losses, which are predominantly due to semiconductor device switching and conduction losses. This work aims to explore machine and converter topologies that result in significant reductions of these converter related losses. The proposed drive topologies are based on the Current Source Inverter (CSI) based technology. Before discussing the proposed topologies in detail a brief review of the CSI based drives is given and contrasted with the Voltage Source Inverter (VSI) based technology.

2.2 Current Source and Voltage Source Converters

The converter topologies can be grouped into two distinct categories depending on the type of energy storage component used in the converter dc link. Current source based topologies employ an inductor as the energy storage element whereas voltage source based topologies employ capacitors as the energy storage elements on the dc link.

2.2.1 Current Source Converter Topology

The current Source Converter (CSC) technology is widely used in industry for medium voltage drives. Figure 2.1 shows a schematic of the CSC drive topology. The CSC drive system comprises of; input filter capacitors C_g on the main ac input, a Current Source Rectifier (*CSR*), a dc link inductor L_{dc} (energy storage element), an output Current Source Inverter (*CSI*) and output filter capacitors C_m which connect to the machine. Current source based drive topologies using both PWM based inverters and Line Commutated Inverters (LCI) are in wide use in industry today. The PWM based CSC are mainly used in power levels up to 10MW whereas LCI based inverters tend to be employed for higher power ratings up to 100MW. Whole wafer power electronic switching devices such as Thyristors, Gate Turn Off Thristors (GTO), Gate Commutated Thyristors (GCT) are used with switching frequencies ranging from machine fundamental frequency for LCI topologies up to 500Hz for the PWM

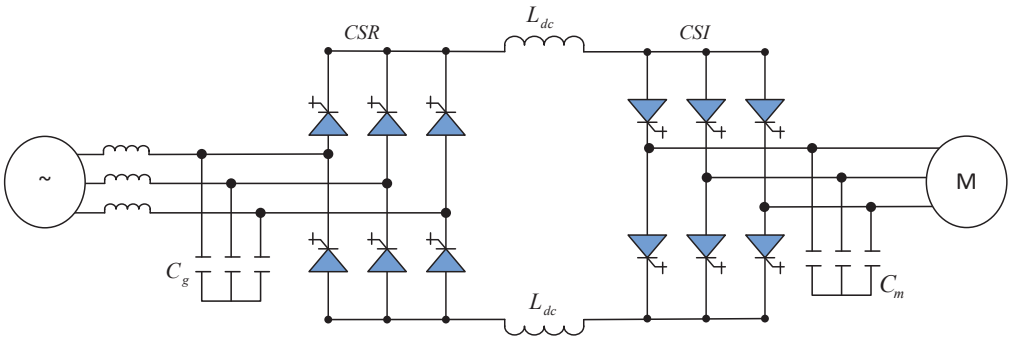

Fig. 2.1 Current Source Converter Topology

topologies. The restriction in switching frequency is due to the high thermal resistance of the Thyristor based semiconductor (GCTs) devices which prevent efficient heat transfer from the devices to the heatsink. Additionally, the restriction on switching frequency helps to minimise the converter switching losses and increase its efficiency. Current source converter topologies for both dc and ac connected drive systems are widely reported in literature [[59–61], [62], [63], [64], [65]] *et-al* and will not be discussed in detail here, only the key advantages and limitations of this topology will be highlighted. The main desirable characteristics of the CSC based drive topologies are:

- **Output Voltage Waveform**: Typical output voltage waveforms from the CSI are suitable for insulation ratings of standard machines and transformers. The output voltage waveforms are near sinusoidal and do not contain high $\frac{dv}{dt}$ which pose increased stress on machine insulation and increased common mode noise. Owing to the very low $\frac{dv}{dt}$ there is no restriction on cable length to the machine as is typical for VSC based systems where voltage reflections along cables can result in voltage doubling effects due to the high $\frac{dv}{dt}$ converter output voltages.

- **Short Circuit Protection**: In case of short circuits on converter output or shoot through faults, the rate of rise of output current is limited by the dc link inductor which allows sufficient reaction time for the CSR controller to rapidly quench the fault current by producing a negative dc link voltage to rapidly force the fault current to zero.

- **Four Quadrant Operation**: This topology has inherent full four quadrant operation, where the power reversal is conveniently achieved by reversing the dc link voltage polarity with no additional hardware requirement.

- **Low device switching frequencies**: Owing to the low switching frequencies, CSC topology is attractive for very high power applications up 100MW where the voltage source inverters normally cannot compete in terms of the cost and energy efficiency of the system.

The main limitations of the CSC topology are:

- **Harmonics and Torque Pulsations**: A consequence of the inherently low device switching frequency is the presence of harmonics on both the input and machine side that can be detrimental to system operation if not carefully evaluated and accounted for at the design stages. The detrimental effects of these harmonics include; increased harmonic losses on the machine as well as increased low frequency machine output torque pulsations which can excite mechanical resonant modes leading to increased stresses on the mechanical drive system. For cost and footprint reasons, the dc link inductor size is often not big enough to provide perfect decoupling between the network and machine side converters. This results in both integer and non integer harmonics being fed back to the ac supply. Often passive filters are necessary to absorb these unwanted harmonics or multi-winding transformers are employed to cancel these unwanted harmonics adding cost to the overall drive solution.

- **Limited Dynamic Performance**: Owing to the use of a dc link reactor which limits the rate of rise of dc link current, the dynamic performance of this drive topology is limited. As a consequence this topology is not used for applications that require very high dynamic performance.

- **LC Resonant Modes**: In this topology, resonant modes exist between the input and output filter capacitances and the respective ac network and machine inductances. The filter capacitors have to be sized to ensure that the LC resonant frequencies are lower than the lowest harmonics produced by the converter,

which often results in increased filter size. The increase in filter size can however be mitigated by employing active damping control schemes which aim to synthesise artificial damping resistance via the control scheme to effectively damp these resonant modes. This however comes at the expense of control modulation margin which has to be reserved for this active damping algorithm.

2.2.2 Voltage Source Converter Topology

The Voltage Source Converter (VSC) technology is widely used in industry for low and medium voltage drives. Figure 2.2 shows a schematic of the VSC drive topology. The VSC drive system comprises of an input PWM filter PWM_{Filter} and PWM ripple current limiting reactor L_{pwm} on the main ac input, an input rectifier VSR which can be in the form of a diode rectifier or Thyristor rectifier or Active Front-End rectifier (AFE), a dc link capacitor C_{dc} (energy storage element) that provides low-impedance voltage source characteristics at the inverter's input, an output PWM inverter VSI which connects to the machine. Very fast switching power electronic devices such as

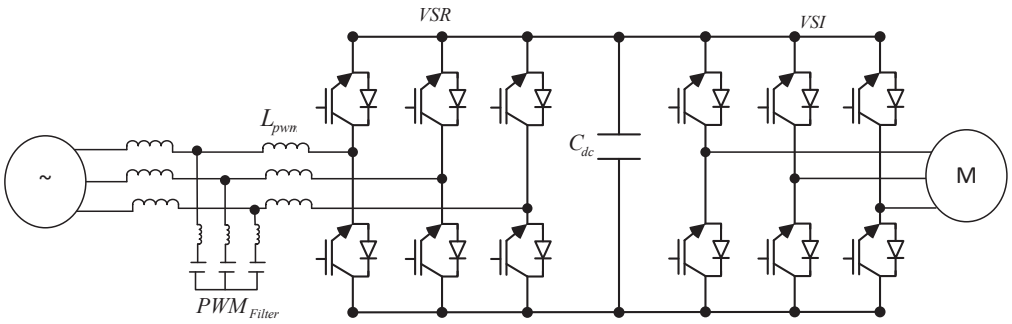

Fig. 2.2 Voltage Source Converter Topology

MOSFETs and IGBTs are employed owing to the high PWM switching frequencies of several kilo-Hertz often used in VSC drive systems. Often passive ac line filters are required to absorb the high frequency PWM harmonics generated by the AFE rectifier. The size of the ac filter is often dictated by the PWM frequency employed, higher PWM frequencies result in smaller ac filter footprint. Often, a tradeoff is required on the choice of switching frequency between minimizing input filter size and converter switching losses. On the machine side, the machine reactance is in general sufficient

to effectively filter the output inverter PWM voltage and yield very good sinusoidal motor current waveform. As a result, output sinewave filters are rarely used with VSC fed machines and very low torque pulsations can be achieved if the PWM switching frequency is sufficiently high, 1-5kHz being typical for high power drives.

Owing to the use of a dc link capacitor, the capacitors provide the instantaneous current to the inverter required in high dynamic systems, and therefore enables high bandwidth current control of the VSC topology. As a consequence, this topology is widely used in applications that require high dynamic performance. Unlike CSC fed drives, the converter output voltage is independent of machine load conditions and is dependent on the dc link voltage and PWM modulation depth.

A key drawback of the VSC topology is the high $\frac{dv}{dt}$ of the synthesised PWM voltage waveforms which requires higher insulation systems on machines and transformers connected to the VSC drive system. Another undesirable consequence of the high $\frac{dv}{dt}$ is the increased common mode currents which can cause system Electro-Magnetic Interference (EMI) issues if not adequately addressed.

In comparison to VSC drive topology, the CSC drive generally features simple converter structure, motor friendly waveforms, inherent four-quadrant operation capability and reliable fuseless short-circuit protection. However, the cost, size, and weight of electrolytic capacitors employed in VSC tend to be significantly lower than DC link inductors employed in comparably rated voltage and current source configurations. Furthermore, new generations of gate-controlled power switches that lack reverse voltage blocking capability tend to be more naturally suited to voltage source inverter requirements. As a result, current source inverters are generally reserved for special applications such as high power drives which can benefit from the Thyristor type whole wafer power electronics devices that have high current handling capabilities.

In all dc systems, the generator ac output is converted to dc by power electronic converters. Even in classical dc generators, the role of the power electronic converter is done by passive brushed mechanical Commutators/converters. For electrical power generating machines whose output ac is rectified to feed a dc bus as is typical in dc systems, the nature of the dc fault current depends on the converter power electronics topology and characteristics of the generating electrical machine. Having alluded to the need for converter fault current limiting capability in dc systems, the IGBT based

VSC type topologies widely used in industry have a major drawback when used in ac/dc conversion stages of the generators. The PWM VSC freewheel diodes rectify the generator output and cannot be switched off, therefore the fault current magnitude is initially defined by the generator impedances and the subsequent duration of the fault is defined by de-magnetisation characteristics of the generator. On the other hand, a CSC topology on the generator output employing power electronic devices with current turn off capability can interrupt the fault current. From the fault current limiting perspective, CSC topology is an attractive choice and it lends itself well to generators ac/dc conversion stages for dc systems. Similar CSC systems have been used in the Thyristor based HVDC transmission systems. The desirable features of CSC topologies have not been fully appreciated and exploited in dc power generation and delivery systems. Further research in CSC based generator/converter topologies can potentially yield significant benefits in terms of alleviating or better still eliminating the stringent operational duty requirements on protection switchgear in dc systems.

The topologies presented in this work are all based on the CSC drive topology. It will be shown that the proposed topologies presented in this work addresses some of the drawbacks of CSC topologies presented above, such as harmonics & torque pulsations, LC resonant modes and limited dynamic performance. Each of the machine topologies considered in this work consists of a plurality of coils in the machine stator winding slots that form a plurality of stator/armature phases and a rotor which comprises of a number of magnetic poles. The machine topologies are essentially DC machines turned inside out with the traditional mechanical commutators replaced by actively controlled electronic commutators. A schematic diagram of a current source fed conventional mechanically commutated dc machine is depicted in in figure 2.3. The armature circuit employ mechanical brushes for current commutation. Unlike conventional brush-less DC machines, this topology features: a high number of stator phases (12, 15, 24 phases and even higher), and is current source fed with electronic commutator power devices that switch at the very low machine fundamental frequencies rather than the high Pulse Width Modulated frequencies of most conventional drives.

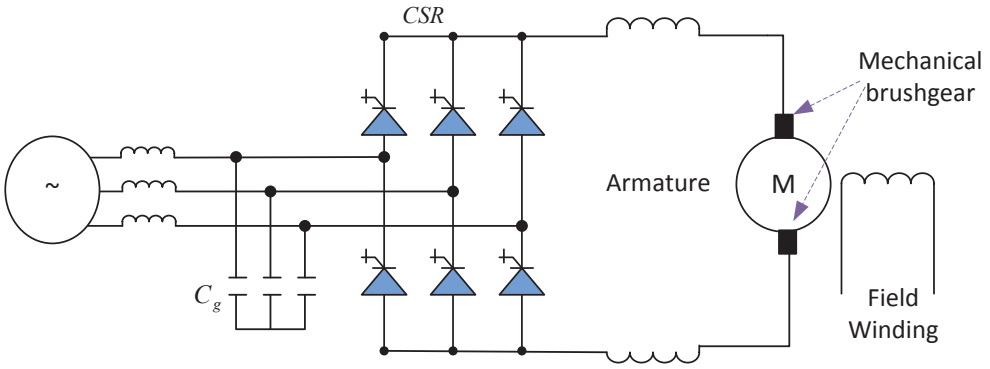

Fig. 2.3 Schematic Diagram of current source fed brush commutated dc machine

2.3 Brush Commutated DC Machines

Figure 2.4 shows the mechanical commutator of a typical brush commutated dc machine.

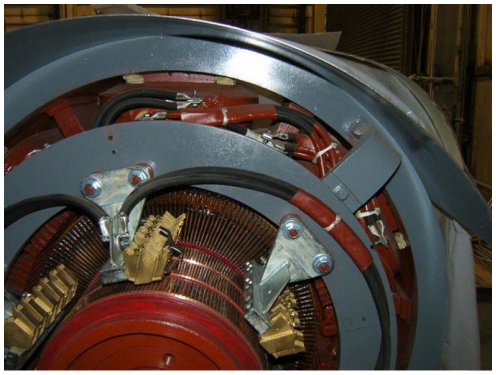

Fig. 2.4 DC Machine Mechanical Commutator

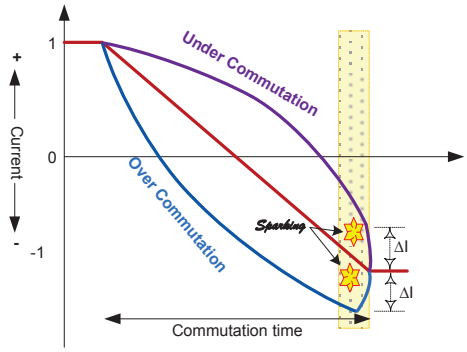

Fig. 2.5 Mechanical Over Commutation & Under Commutation

In brush commutated dc machines, the machine's armature current commutation is facilitated by the armature coil voltage. This requires the brush position to be set to allow sufficient time for the current to be reduced to near zero by the time an outgoing commutator segment breaks contact with the trailing edge of the brush to avoid arcing (under-commutation) as depicted in figure 2.5. Furthermore, the brush position must be set to avoid excessive time for current reduction and subsequent current reversal by the time an outgoing commutator segment breaks contact with trailing edge of the brush to avoid arcing (over-commutation), as shown in figure 2.5. Both under-commutation

and over-commutation are typically destructive and in large dc machines inter-poles are often employed to mitigate the risk of commutator flash-over at the expense of size and complexity of the machine. These mechanical commutator drawbacks often result in large and complex rotating mechanical commutators and often impose a restriction on the maximum machine operating speed and machine rated voltage, typically to less than 1 kV. The machine topologies considered here circumvent the limitations of the mechanical commutator brush-gear by employing power electronic means of armature current commutation. Figure 2.6 shows a schematic of the layout of mechanical and electronic commutation topologies. The benefits of electronic commutation are highlighted by contrasting the commutation stages of mechanical and electronic commutation.

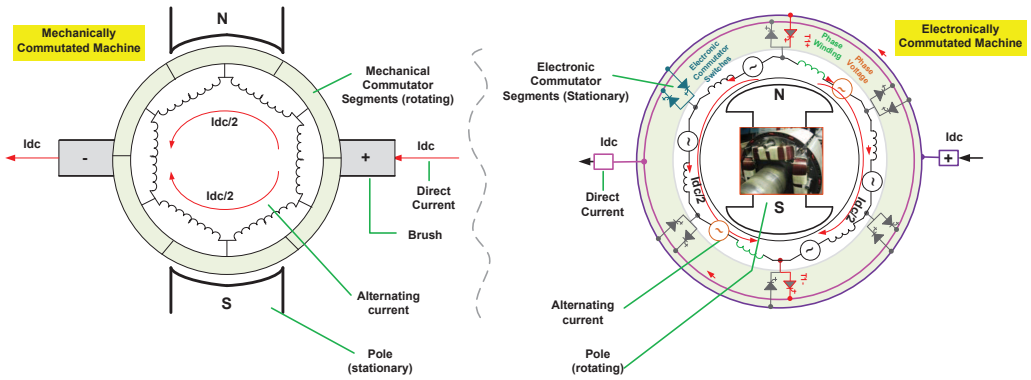

Fig. 2.6 Schematic Diagram Showing Comparison of Mechanical & Electronic Commutation

2.4 Mechanical Commutation

The operating principles of mechanically commutated dc machines is widely published [[35], [66], [67]]. Only operating principles that are relevant for contrasting with electronic commutation will be repeated here for clarity. For brush commutated dc machines, the mechanical commutation process is depicted by three stages highlighted in figure 2.7 for the ideal case where brush and commutator segment width are equal, i.e., there is only one commutator segment per armature slot. Stage 1 is before the current commutation, where all the current is going through commutator segment 1. Each machine phase winding carries half of the total current that is going through the

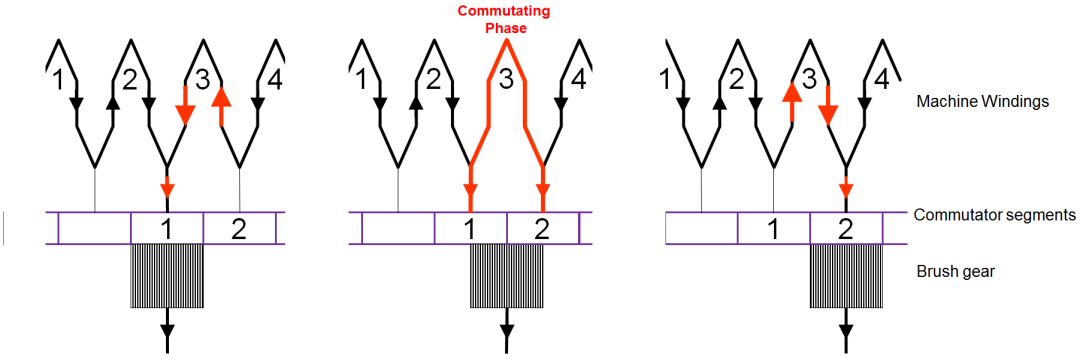

Fig. 2.7 Mechanical Commutation Process

commutator. Stage 2 occurs during commutation when the brush makes contact with adjacent commutator segment 2 thereby shorting the commutating phase. The current in the commutating phase reduces to zero and eventually reverses polarity as the rotor continues to move relative to the armature. Stage 3 depicts the state when the current commutation is complete, i.e. when the current in the phase undergoing commutation has completely reversed and the brush is in contact with segment 2 only. Undesirable brush wear and sparking can occur due to over-commutation or under-commutation as illustrated in figure 2.5 if the current reversal is too fast or too slow respectively. The energy dissipated as heat during the sparking is given by:

$$E = L_c \frac{\Delta I^2}{2} \tag{2.1}$$

where, L_c is the phase commutating inductance and ΔI is the current change/jump at the end of the commutation as illustrated in figure 2.5.

2.5 Electronic Commutation

The electronic commutation process is depicted in a simplified sequence shown in figure 2.8, and is closely related to but not the same as that of the classical brush commutated dc machine above. Stage 1 depicts the state just before commutation where all the current is going through the switching device T1. Stage 2 starts when the device T2 is turned ON to initiate the current commutation. At this stage both switching devices T1 & T2 are ON, thereby effectively short circuiting phase 3 undergoing commutation. At this stage the current starts reducing in switching device

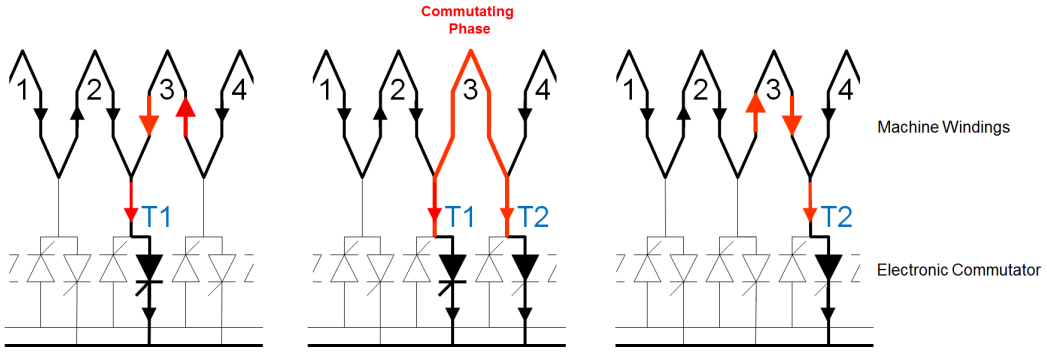

Fig. 2.8 Electronic Commutation Process

T1 and increasing in switching device T2 and will eventually reverse polarity in the commutating phase. Stage 3 depicts the state when the commutation process has ended and phase current reversal has been completed in phase 3 and device T1 is switched OFF. The undesirable effects of under-commutation or over-commutation encountered in brushed commutators are eliminated when electronic means of current commutation is employed. The electronic commutator can tolerate over-commutation without sparking because the commutator power semiconductor switching device reverse recovery blocks the current reversal that would otherwise be interrupted by brush commutator action. Furthermore, the electronic commutator power devices can tolerate under-commutation without sparking as the gate turn off process displaces the sparking that would otherwise occur in mechanical commutators.

Additionally, the electronic commutation process offers more flexibility because power semiconductor devices can accommodate far greater voltages than can be supported between classical DC machine commutator segments. This characteristic of electronic commutation is attractive particularly for high power machines as it allows machines with higher voltage ratings to be realised. This can yield smaller footprint, lighter and more cost effective machines as less copper or aluminium is required for a given power rating owing to the increased operating voltage. Furthermore, an additional degree of freedom inherent in electronic commutation is that the position at which current is injected into the stator relative to the rotor position (similar to brush position) can be freely controlled to enhance the four quadrant operational capability and dynamic performance of the machine. This will be discussed later in detail in the control aspects of this drive topology.

2.6 Multiphase DC Machine Topologies

Having alluded to the benefits of electronic commutation in dc machines, this chapter now shows that there are additional degrees of freedom that can further be exploited to yield machines that meet specific target application requirements. For example, in applications where the drives are decoupled from the ac grid, such as, aircraft power systems, marine power systems & automotive drives and dc power supply systems, there is no requirement for adhering to the standard three phase machine topology.

Increasing the machine phase number beyond three enhances machine harmonic performance due to the consequential decrease in detrimental low order space and time harmonics that give rise to undesirable torque pulsations and mechanical resonance issues [[41], [40], [42], [47]]. In other words, rather than trying to reduce the amplitude of space and time harmonics individually, increasing the motor phase number gives less interaction between time and space harmonics, which improves the quality of the airgap flux. Therefore, if the phase number is sufficiently increased it is possible to obtain good motor performance regardless of winding design or supply waveforms [68], [69]. As alluded to earlier, by increasing the phase number, the unwanted harmonics are pushed to higher orders where their amplitudes diminish in inverse proportion to their order [70].

2.6.1 MMF Harmonics for Multiphase Stators

The machine stator mmf harmonics can be analysed using Fourier series as in [[70, 71],[40], [72]]. For purposes of highlighting the benefits of increased phase number on the stator mmf harmonics, let us consider a single phase winding of full pitch such that the winding function for the stator and rotor can be represented as shown in figure 2.9. By assuming each stator coil winding function to be an odd symmetric squarewave function implies that only odd space harmonics can exist. If the stator coil winding is placed on the stator and with an offset of α_s radians around the stator relative to a given reference axis, its stator phase coil winding function can be derived from the general Fourier transform for a squarewave and represented in equation form by:

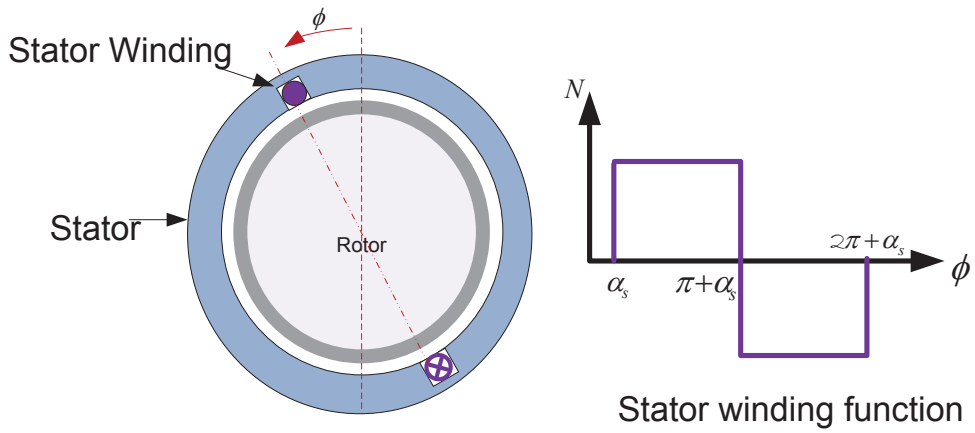

Fig. 2.9 Single Fully Pitched Stator Winding

$$N_s(\phi) = \sum_{j=1}^{\infty} b_{S_j} \sin(j(\phi_s + \alpha_s) \tag{2.2}$$

where, ϕ is the angular position along the stator inner surface, $\alpha_s = 2\pi/N$ is the stator phase coil position offset, N is number of stator phases, b_{Sj} are the Fourier coefficients of $N_s(\phi_s)$ such that;

$$b_{S_j} = \frac{2N_w}{\pi j} \sin(\frac{\pi j}{2}) \tag{2.3}$$

where N_w is coefficient of winding function. For machine topologies being considered in this work, the stator winding current is typically a squarewave function. The stator current injected by a dc supply and commutated by the stator can also be expressed as a Fourier series by;

$$i_s(t) = \sum_{k=1}^{\infty} b_{T_k} \sin(k(\theta_s + \delta_s) \tag{2.4}$$

where, $\theta_s = \omega t$ is the angular frequency of the fundamental current waveform and δ_s is the phase of the stator current waveform. The Fourier coefficients b_{Tk} are given by;

$$b_{T_k} = \frac{1}{\pi j} \int_0^{2\pi} i_s(t) \sin(\omega t) dt \tag{2.5}$$

By multiplying (2.2) and (2.4), the stator mmf $F_s(\phi,t)$ produced by a single coil with a winding function $N_s(\phi)$ carrying a current $i_s(t)$ is obtained. This can be expressed as:

$$F_s(\phi,t) = N_s(\phi)i_s(t) \tag{2.6}$$

Since we are considering machine topologies with a plurality of stator phases N, where N is significantly greater than three, the above formulation can be extended to a generalised machine with N stator phases that are equally phase displaced by $2\pi/N$ radians around the stator. The total stator mmf for this N phase windings can be computed by substituting (2.2) and (2.4) into (2.6) and summing the contributions due to all the N phases. To keep the number of turns in the stator constant, each winding has $\frac{1}{N}$ as many turns as a single winding. The total mmf considering stator phases $a = 1$ to $a = N$ can be expressed as:

$$F_s(\phi,t) = \sum_{a=1}^{N}\sum_{j=1}^{\infty}\sum_{k=1}^{\infty}\frac{1}{N}b_{S_j}b_{T_k}\sin(k(\theta_s+\frac{\pi}{N}a))\sin(j(\phi_s+\frac{\pi}{N}a)) \tag{2.7}$$

Equation 2.7 can be simplified by applying the product to sum trigonometric identity;

$$\sin(u)\sin(v) = \frac{1}{2}[\cos(u-v)-\cos(u+v)] \tag{2.8}$$

Applying the identity (2.8) to (2.7) and simplifying gives;

$$F_s(\phi,t) = \sum_{j=1}^{\infty}\sum_{k=1}^{\infty}\frac{1}{2N}b_{S_j}b_{T_k}\sum_{a=1}^{N}[\cos(k\theta_s - j\phi_s + \frac{\pi}{N}(k-j)a) - \cos(k\theta_s + j\phi_s + \frac{\pi}{N}(k+j)a)] \tag{2.9}$$

To better visualise the implication of (2.9), a close inspection reveals that this equation can be simplified further by splitting it into a pair of rotating harmonic mmf waveforms, one rotating in the positive direction and the other rotating backwards as;

$$F_s(\phi,t) = \begin{cases} +\sum_{j=1}^{\infty}\sum_{k=1}^{\infty}\frac{1}{2}b_{S_j}b_{T_k}\cos(k\theta_s - j\phi_s) & \text{when } k-j = 0,\pm 2N,\pm 3N,... \\ -\sum_{j=1}^{\infty}\sum_{k=1}^{\infty}\frac{1}{2}b_{S_j}b_{T_k}\cos(k\theta_s + j\phi_s) & \text{when } k+j = 0,\pm 2N,\pm 3N,... \end{cases} \tag{2.10}$$

It can be seen from (2.10) that increasing the number of phases N leads to fewer possible combinations of space j and time k harmonics that satisfy the equation (2.10), as a consequence there are fewer harmonic components in the two rotating fields. it is also clear from this equation that the higher the stator phase number N , the higher the space and time harmonics that can exist in these fields. Bearing in mind that the amplitude of a harmonic varies inversely with its order, the above observations imply that increasing the stator phase number shifts the remaining undesirable harmonics to higher orders where their undesirable impact on machine performance diminish with increasing stator phase number. The same analysis can be extended and also holds for the rotor circuit for machines with multiphase stator windings.

2.7 Multiphase Stators and Power Electronics Integration

A Large number of stator phases also facilitates the electronic commutator and power electronics cooling design when integrated into the machine due to increased per phase surface area around the periphery of the machine stator as shown in figure 2.10. As such, the topology of the machine and its electronic commutator can be optimised as a self-contained system.

In general the rating and dimension of the machine are related by:

$$NV_sI_s = \frac{\pi^2}{\sqrt{2}}D^2L_A(AB_g)(W_f)\Omega \tag{2.11}$$

where, N is number of stator phases, V_s and I_s are fundamental rms stator voltage and current, D is armature diameter (m), L_A is effective armature core length (m), A is

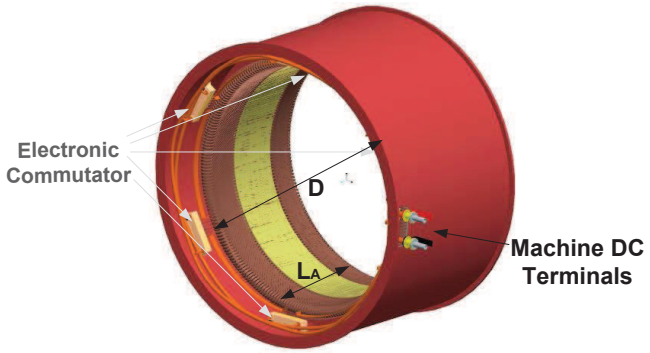

Fig. 2.10 3D Illustration of Machine Stator with Integrated Electronic Commutator

armature current sheet density ($A.m^{-1}$), B_g is the amplitude of the first harmonic flux density (T), W_f is the winding factor (pitch and distribution) and Ω is revolutions per second. Increasing the number of stator phases reduces the phase currents proportionally, owing to the reduced per phase VA rating. This facilitates both electronic commutator and machine design and manufacturing.

Another degree of freedom that derives from the high phase number approach is the choice of machine and converter topology. Two types of machine topologies are possible depending on how the power electronic commutating devices are connected to the machine stator phases. These two types will be referred to as *two-level* and *multi-level* machine/converter topologies.

2.8 Two-Level Converter/Machine Topology

The 2-level machine/converter topology and its associated electronic commutation process is described in detail in [73]. The machine has a stator winding that includes a plurality (significantly larger than 3) of uniformly phase displaced stator phases and a rotor winding. Adjacent stator phase windings are connected in the ac domain to form a polygonal machine winding. The individual stator windings are also connected to power electronic switching modules as highlighted in figure 2.11 forming a 2-level converter/machine topology where each machine phase winding terminal is sequentially connected to the positive ($+V_{dc}$) and negative ($-V_{dc}$) machine dc poles through the electronic commutator phase switches, hence the 2-level topology. In

figure 2.11 any power electronic device with reverse voltage blocking capability can be employed in this topology.

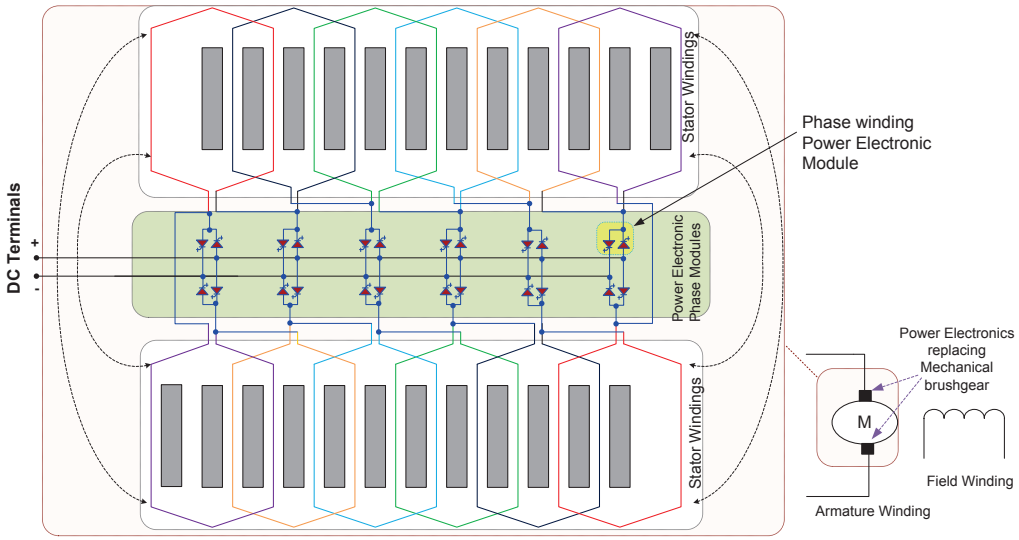

Fig. 2.11 2-Level Topology: Stator Phase winding Circuits and Power Electronics Topology

2.9 Multi-level Machine/Converter Topology

In applications where high machine output voltages are required, the 2-level topology highlighted in figure 2.8 may not be desirable. A possible shortcoming of the 2-level machine topology is that the machine/converter topology does not lend itself well for high voltage dc generating systems since this will require the use of series connected semiconductor switching devices and addressing all the issues associated with static and dynamic voltage sharing across the series connected devices. Furthermore, since each machine armature winding phase terminal is sequentially connected to the positive and negative dc terminals, the dominant insulation stress is ac and demands a higher machine armature insulation level. For high voltage applications, an alternative multilevel, multiphase machine/converter topology is more attractive.

Similar to the 2-level topology, the multi-level topology features a large number of stator phases. The stator winding comprises of a plurality of coils in the winding slots forming a plurality of stator phases significantly greater than three. Unlike the 2-level topology above where the connections between adjacent stator phases

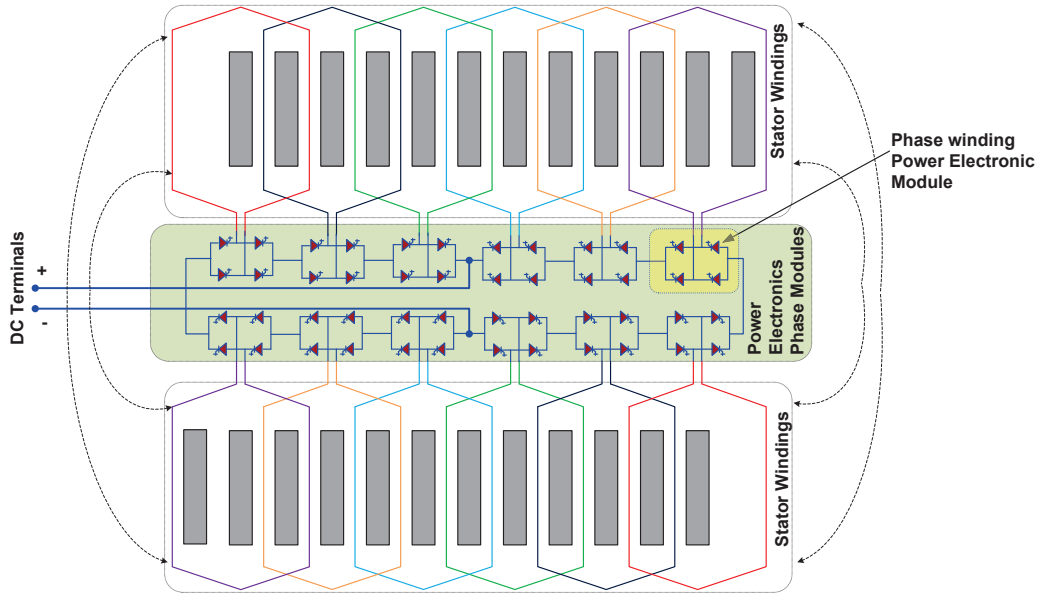

Fig. 2.12 Multi-Level Topology: Stator Phase winding Circuits and Power Electronics Topology

form a continuous polygonal winding in the ac domain, each stator phase winding is terminated in a power electronic switching module and connects to the adjacent stator phase winding in dc domain through the dc output terminals of the power electronic switching module as highlighted in figure 2.12. The series & parallel connected switching modules form a multi level converter/machine structure where each machine phase winding sequentially connects to the module output positive ($+V_{dc}$) and negative ($-V_{dc}$) poles through its switching power electronic modules. Each switching module's dc voltage is only a small fraction of the total machine's output dc link voltage and is inversely proportional to the number of stator phases' switching modules connected in series, hence the multi-level topology. The two end terminals of a plurality of seriesed switching module sections can be connected in parallel with one or more similar sections to form the overall machine dc output terminals. For example, figure 2.12 depicts the case where two sets of switching sections, each with six switching phase modules in series, are connected in parallel to the two dc output terminals of the machine. Each power electronic switching module mimics a single phase H-Bridge topology. Power switching devices with reverse voltage blocking and gate turn off capabilities are applicable for the electronic commutator.

2.10 Summary

This chapter has briefly introduced the multiphase electronically commutated dc machine topology. The similarities and differences between conventional mechanical brush current commutation and electronic current commutation together with some key advantages of electronic means of current commutation have been presented. Machine MMF analysis presented has highlighted the potential benefits of multiphase topologies in relation to machine harmonics. It has been shown that if the machine stator phase number is sufficiently increased, undesirable low order harmonics are shifted to higher orders where their undesirable impact on machine performance diminish inversely with the harmonic order. The two level and multilevel multiphase electronically commutated dc machines topologies have been introduced. The next chapter will explore the operational principles of two level topology.

Chapter 3

Two Level Multiphase Electronically Commutated DC Machine Topologies

3.1 Introduction

The work reported in this chapter builds on the preliminary earlier work carried out by the author and others on two level multiphase electronically commutated dc machine and converter topology reported in [74, 73, 75, 26]. This chapter will firstly cover some of the background operational characteristics of this topology and then extend the analysis to expose the beneficial operational attributes and constraints of this topology. Based on this analysis, simulation models and control schemes are formulated and implemented to fully characterise the operational behaviour of this topology. The earlier work reported in [74] on the two level topology focused on machines with even number of stator phases. This work further extends the two level topology analysis to multiphase electronically commutated dc machines with odd number of stator phases. The simulation models developed for these two topologies are then used in the comparative analysis of the odd number and even number topologies to fully expose the beneficial attributes and limitations of both topologies.

3.2 Two Level Topologies

Electronically commutated machines that use armature volts to naturally commutate Thyristors or cause forced commutation of Thyristors by reverse recovery have been reported [76], [77], [78], [79], [80]. For example, Line Commutated Inverter (**LCI**) drives have been widely used in industry for high torque density and high efficiency applications. The LCI drives benefit from low switching frequencies and good efficiencies for high power applications as highlighted in a comparative study in [81]. However, they suffer from high low order harmonics and inherent high torque pulsations and high drive train noise and vibration signature [82],[83]. Often large dc link inductors are required to reduce the amplitude of the current harmonics that can cause increased machine torque ripple and harmonic losses. The topologies studied in this work seek to mitigate these undesirable characteristics of these conventional electronically commutated machines.

The two level multiphase topology is not a new concept, in fact, conventional brush commutated dc machines essentially fall into this category, albeit with mechanical means of current commutation. The limitations of mechanical brush commutators have been well documented and summarized in [84],[85] and others. The generation of sparks between the brushes and the segments of the commutator has remained the main limiting factor to the performances of d.c. machines. The most classical solution to the problem has been the use of commutating poles to generate additional emfs to help the inversion of currents in rotor coils at proper time. Earlier work by Bates *et-al* [86, 84, 87, 85] in the 1960s recognised these drawbacks and proposed ways of mitigating them through the use of power electronic devices. However, this earlier work did not focus on complete elimination of mechanical current commutation, rather, it focused on using electronic means to assist the mechanical brush commutation.

Through analysis, modelling and experimental work, the work presented here extends the initial concept of fully electronically commutated multiphase dc machines presented in [74, 73]. Initial focus is given to the topology with an even number of stator phases. An analysis of the operating principle is presented together with simulation and experimental results for this topology. The analysis and modelling work is further extended to cover a new alternative topology with an odd number of

stator phases. Simulation and experimental results of the odd number topology are also presented. The experimental results presented are based on laboratory prototype drives build to validate these topologies. Details of these experimental drives are detailed in later chapters.

The 2-level multiphase electronically commutated dc topology lends itself well to low voltage applications where commercial off the shelf semiconductor devices can be used for current commutation without the need for series connection of the switching arm devices. The 2-level topology can be applied to both dc and ac fed systems for both motoring and generating applications. This topology is a current source fed drive, as such it requires a current source converter to regulate the amplitude of the dc link current.

3.3 Even Stator Phase Number

The even stator phase number topology features a plurality of stator phases connected to form a polygonal machine winding with N stator phases, where N is the number of stator phases and is an even number. It is assumed that all the stator phase windings are phase displaced equally by $\frac{2\pi}{N}$ radians (electrical) and connected internally to form a complete polygonal winding. The terminals of each phase are also connected to the electronic commutator. For example, figure 3.1 depicts a machine with twenty four stator phase windings each phase comprising of a single coil, two rotor poles and a simplified electronic commutator circuit. The connection of all stator phases in a polygonal fashion gives rise to the possibility of undesirable net circulating currets in the machine stator polygonal winding. This is unlikely to occur in this even stator phase number machine topology due to machine symmetry. Owing to the symmetry with even number of stator phases, simple fully pitched stator phase winding function can be employed with no resultant induced circulating currents in the polygon during machine operation. In this chapter, the key distinct characteristics of the even phase number topology are highlighted in relation to their impact on electronic current commutation, power electronics complexity, harmonic performance and commutating inductance.

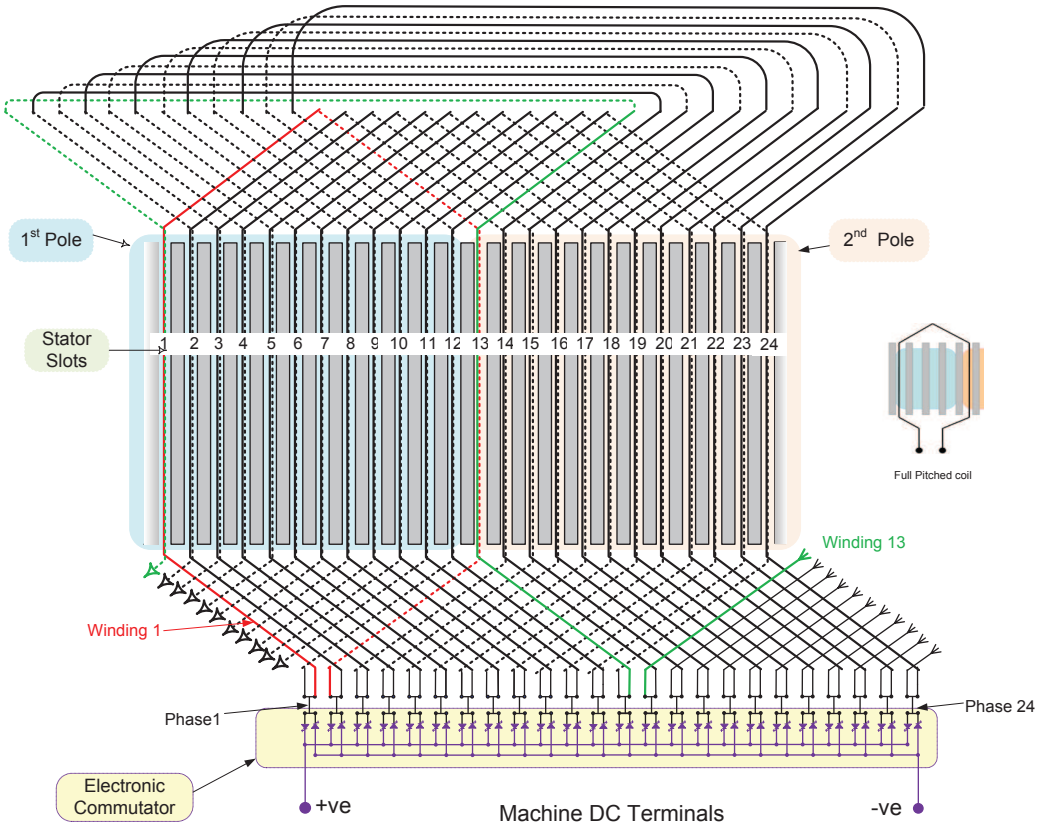

Fig. 3.1 Stator Winding Connections to Electronic Commutator for a 24 Phase Machine

Earlier work by the author and others cited above has dealt with fully electronically commutated dc machine with an even number of stator phases. However, little attention was given to the simulation and analysis of the current commutation process and control challenges posed when electronic commutation is employed to replace mechanical means of current commutation. Some of the key challenges and questions that had to be addressed included; (a) can suitable control schemes be formulated to enable electronic commutators to mimic the desirable operational attributes of mechanical commutators such as synchronised & safe current commutation control?, (b) can the proposed control strategies match the superior transient, dynamic and steady state performance of classical brush commutated dc machines over the entire four quadrant machine torque/speed range?, (c) what failure modes exist and what design features are needed to enable fault tolerant operation of electronic commutator?, and (d) which machine design parameters have beneficial and detrimental effects on electronic current commutation and how can they be optimised? In order to address some of these challenges, machine models suitable for direct interface to the electronic commutator

power electronic circuit models were developed and used for the simulation analysis and verification work presented in this chapter. Experimental design and validation testing conducted to confirm some of these aspects is presented and discussed in later chapters.

3.3.1 Theory of Operation

To explain the operating principle of the even stator phase topology, figure 3.2 will be used. In this topology the dc link current amplitude is controlled by a current source converter depicted as *supply converter* in this figure. Figure 3.2 also depicts the equivalent mechanically commutated dc machine to expose the similarities and differences between the two machine concepts. It is obvious that the two representations in this figure are functionally the same, but this functionality is achieved by employing completely different means of current commutation.

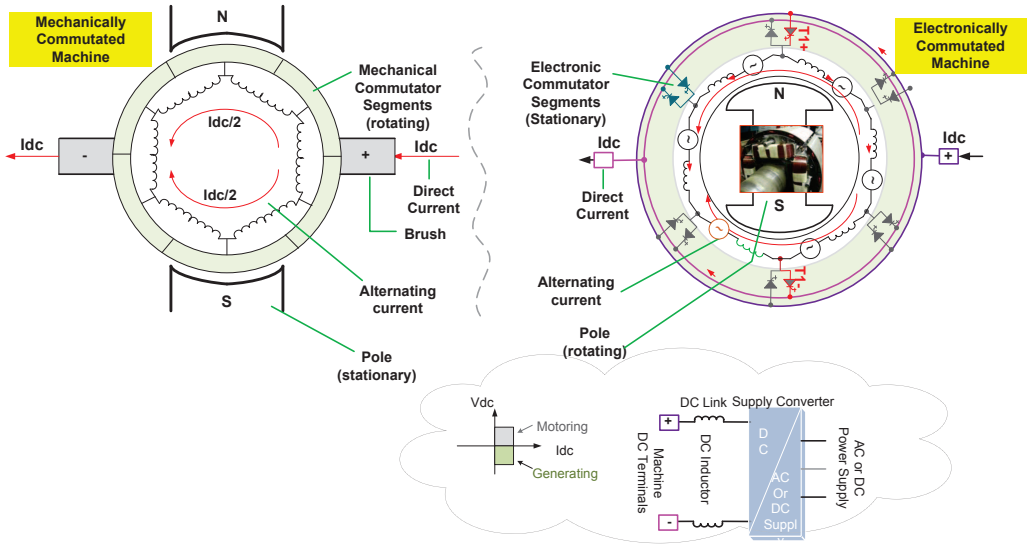

Fig. 3.2 Two Level Machine & Converter Topology: Contrasting Mechanical & Electronic Commutators

The principle of electronic current commutation is based on a rearrangement of the classical dc commutator such that each machine phase winding terminal is connected to two electronic switching devices that sequentially connects the machine phase to either the positive or negative dc poles of the machine dc terminals as depicted in figure 3.2. The electronic switching devices are phase controlled to inject the dc current into

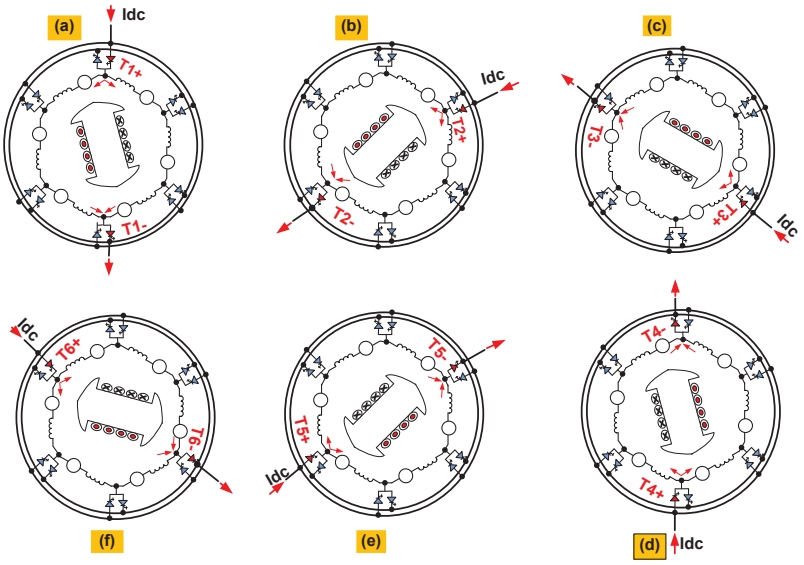

Fig. 3.3 Illustration of Machine Operation States

the machine stator at defined phase positions relative to the rotor position to generate machine torque. For example, figure 3.3 shows a six phase machine and the operating sequence from state (a) to state (f) for a complete mechanical shaft revolution. Unlike brushless dc machines where a given number of stator phases are energised at any given time, here all the stator phases carry current all the time and contribute to the machine torque.

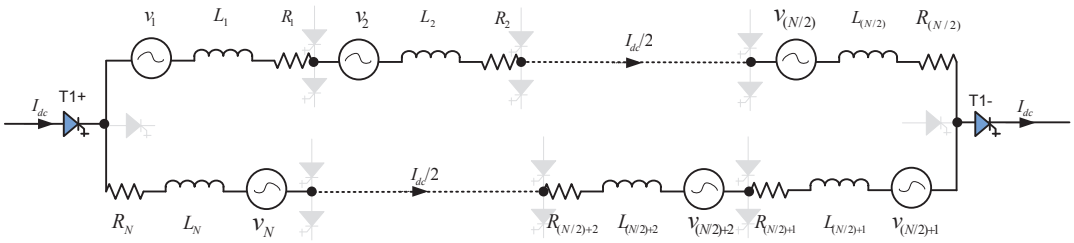

Fig. 3.4 Equivalent Circuit Before Current Commutation

The above operating principle has been extended to cover a more generic case for a machine with N even stator phases. In fact, the generic models and generic electronic commutation control strategies developed in this work have been applied to topology simulations with up to 48 stator phases and experimentally validated on a machine with 24 stator phases. In each of these generic cases, the dc link current is injected into the machine through device T_{n+} connected to the positive dc link pole

and it exits the machine windings through device T_{n-} connected to the negative dc pole, where n is the active pair of commutator phases. Owing to the symmetry of even stator phase number, the current injected via the electronic commutator splits equally between the two halves of the machine polygon as illustrated in figure 3.4. Through simulation and analysis, it has been found that to ensure symmetrical operation of the even numbered machine topology with balanced voltages and currents, the switching of the commutator device pairs T_{n+} and T_{n-} have to be synchronised to occur at the same time intervals.

3.3.2 Current Commutation In Even Numbered Topology

A section of the machine and two adjacent electronic commutator segments depicted in figure 3.5 is used to analyse the current commutation process and also expose extra beneficial degrees of freedom brought about by electronic means of current commutation .

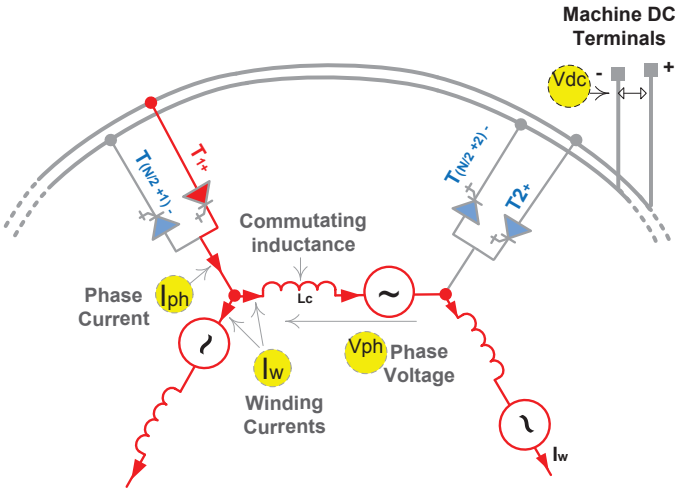

Fig. 3.5 Two Level Machine & Converter Highlighting Machine Signal Definitions

To initiate current commutation from devices T_{1+} and T_{1-} to the next commutator phases, devices T_{2+} and T_{2-} are synchronously turned ON. The effect of turning ON devices $T_{2\pm}$ results in phases 1 and phase *(N/2+1)* respectively being short circuited during current commutation as depicted in figure 3.6. When current commutation is complete, the dc link current will be injected into the machine through device $T_{2\pm}$ of phases 2 and *(*N/2+2) respectively as depicted in figure 3.7.

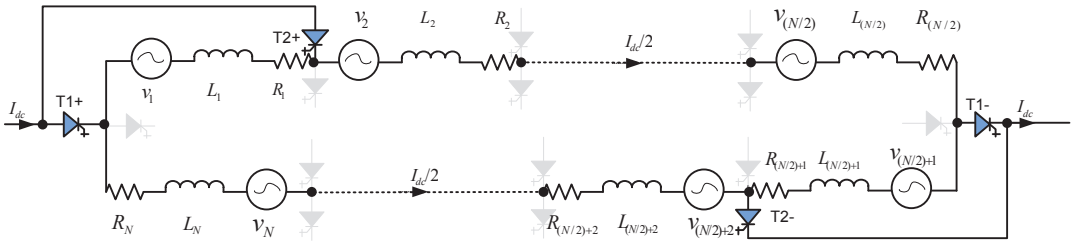

Fig. 3.6 Equivalent Circuit During Current Commutation

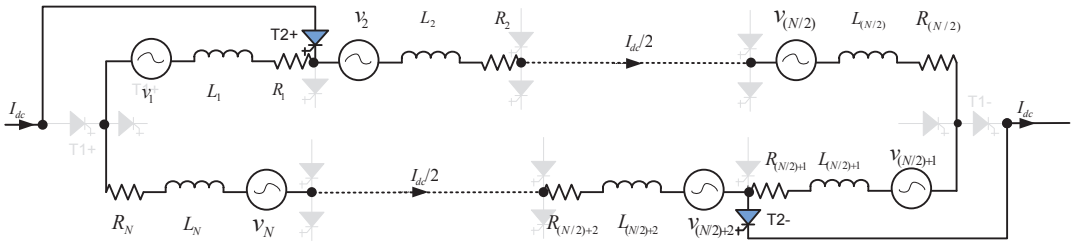

Fig. 3.7 Equivalent Circuit after Current Commutation

Figure 3.8 gives an illustration of the electronic commutator states before, during and after commutation transitions for positive and negative machine shaft speeds. Closer examination of the electronic current commutation process reveals that two current commutation transition stages are possible; (a) **Indirect transition** highlighted as steps *1,2, 3,* .. in figure 3.8 where some intermediate commutation states highlighted in shaded (red) are employed, (b) **Direct transition** highlighted as steps *(a), (b),* .. where no intermediate states are employed between active states. The states highlighted in shaded area (red) are the commutation transition states where for example, the electronic commutator moves from a state when devices (T_{1+}, T_{1-}) conduct the machine current, through a transition state when devices $(T_{1+}, T_{1-}, T_{2+}, T_{2-})$ all conduct current, to a state when the commutation is complete and devices (T_{2+}, T_{2-}) only conduct the machine currents for positive speed. In the case of indirect transitions, for example when devices $(T_{1+}, T_{1-}, T_{2+}, T_{2-})$ are all turned ON, defines the commutation interval. Its clear that by controlling these transitions, the electronic commutator can be operated in *under-commutation* or *over-commutation* modes. Figure 3.9 shows measured waveforms illustrating the indirect state transition between phase 1 and phase 2 commutator devices T_{1+} and T_{2+}

Simulation and experimental results have shown that control of direct and indirect transitions yields an additional degree of freedom that can be used to optimise the

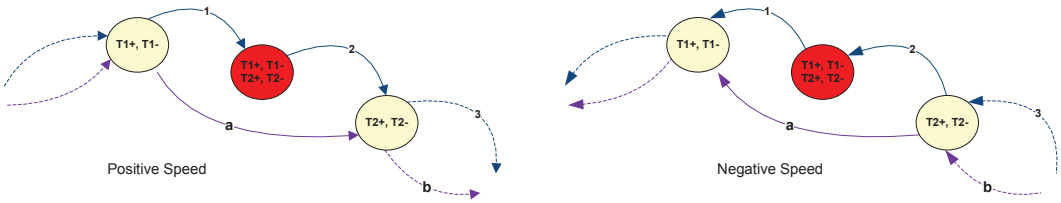

Fig. 3.8 Electronic Commutator Devices State Machine

design and operational characteristics of the electronic commutator. In essence, this equates to variable overlap interval between commutator brush positions in conventional brush commutated dc machines. This degree of freedom does not exist in the mechanically brush commuted dc machines since commutator brush position can not be dynamically varied and is usually fixed. Simulations and experimental tests have shown that this extra degree of freedom has a significant impact on both the power electronics design in terms of the switching devices & snubber circuits ratings and also on the overall drive performance in terms of output dc voltage regulation, efficiency and fault tolerance capabilities.

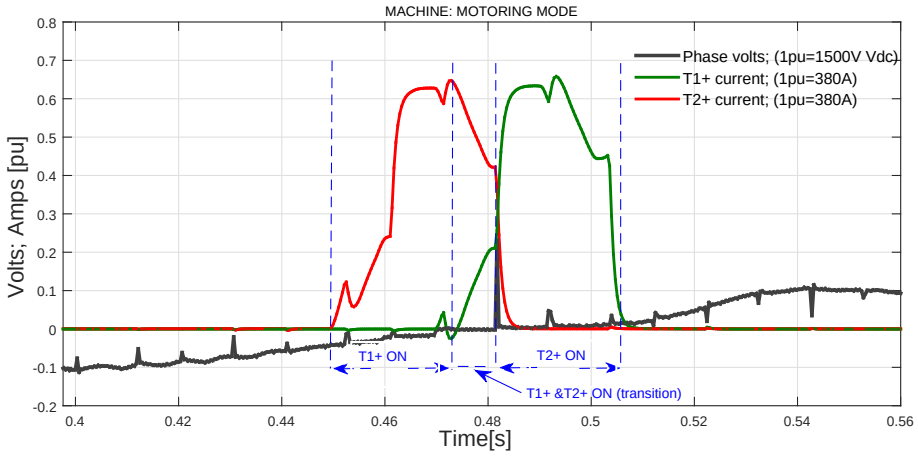

Fig. 3.9 Measured Waveforms of Indirect State Transition for Commutator Phases 1 & 2 Devices T_{1+}, T_{2+}

Figure 3.10 shows the truth table of permitted combinations of commutator device states for positive and negative shaft speeds, where T_{N+} signify commutator device that connect the machine N phase winding to the positive dc terminal and T_{N-} connects the winding to the negative dc terminal respectively. The "1" in the diagonal elements represent the active states of the commutator when not undergoing commutation.

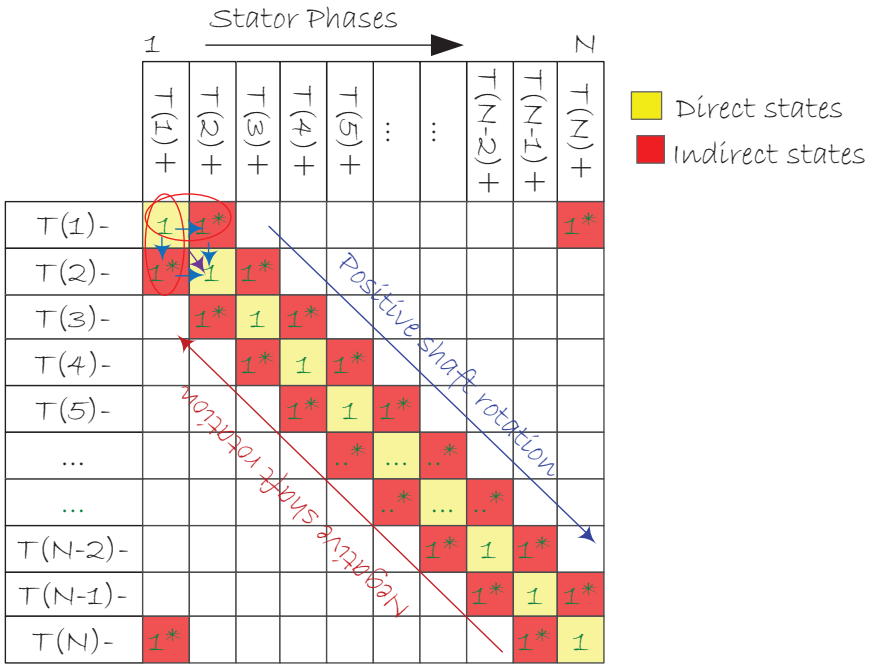

Fig. 3.10 Electronic Commutator Device States Truth Table

The "1*" indicate the indirect transition states between commutator segments during current commutation as illustrated in figure 3.8 .

3.3.3 Electronic Commutator Current Commutation Analysis

The current commutation process can be analysed with the help of figure 3.11 which shows how the dc link current $I_{dc}(t)$ divides into $i_1(t)$ and $i_2(t)$ when commutating current from device T_{1+} to T_{2+}. Notice winding phase current $i_3(t)$ will have reversed polarity at the end of the current commutation process.

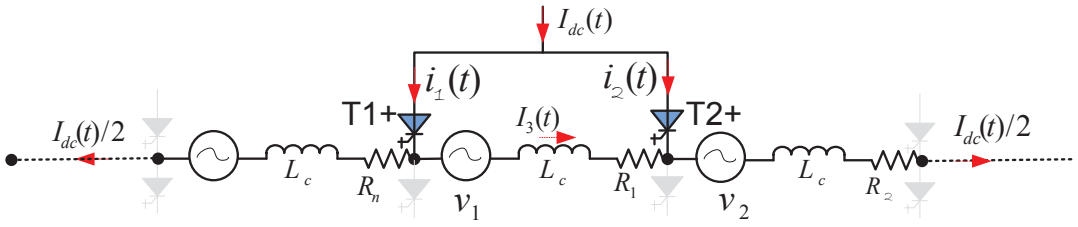

Fig. 3.11 Circuit Diagram of Commutating Phase

Applying Kirchhoff's voltage and current laws imply;

$$v_{T1}(t)+v_1(t)+L_c\frac{di_1(t)}{dt}+R_1i_1(t)-R_1i_2(t)-L_c\frac{di_2(t)}{dt}-v_{T2}(t)=0 \tag{3.1}$$

and

$$I_{dc}(t)=i_1(t)+i_2(t) \tag{3.2}$$

where, v_{T1} & v_{T1} are the device 1 & 2 on state voltage drops respectively, $v_1(t)$ is the machine phase 1 voltage, $i_1(t)$ & $i_2(t)$ are the commutator phase 1 & 2 device currents, L_c is the commutating inductance and R_1 is the phase resistance. Assuming dc link current is constant implies;

$$\frac{di_1(t)}{dt}=-\frac{di_2(t)}{dt} \tag{3.3}$$

Expressing (3.1) in terms of dc link current and device T_{1+} current gives;

$$v_1(t)+R_1(2i_1(t)-I_{dc}(t))+v_{T1}(t)-v_{T2}(t)=-2L_c\frac{di_1(t)}{dt} \tag{3.4}$$

where $v_{T1}(t)$ and $-v_{T2}(t)$ are the commutator device voltage drops.

The commutation interval γ can be obtained by solving (3.4), i.e;

$$\int_0^{\gamma}\Big(v_1(t)+R_1(2i_1(t)-I_{dc}(t))+v_{T1}(t)-v_{T2}(t)\Big)\,\mathrm{dt}=\int_{I_{dc}}^{0}(2L_c)\,\mathrm{di_1(t)} \tag{3.5}$$

If the switching device voltage drops (v_{T1},v_{T2}) and the armature phase winding resistance R_1 are negligible, equation (3.4) can be simplified to give;

$$\int_0^{\gamma}v_{pk}\sin(\omega t)\,\mathrm{d}(\omega\mathrm{t})=\int_{I_{dc}}^{0}(-2L_c\omega)\,\mathrm{di_1(t)} \tag{3.6}$$

assuming;

$$\frac{di}{dt}=\frac{di}{d(\omega t)}.\frac{d(\omega t)}{dt}=\omega\frac{di}{d(\omega t)} \tag{3.7}$$

and;

$$v_1(t)=V_{pk}\sin\omega t \tag{3.8}$$

where V_{pk} is the peak armature voltage.

The solution for the commutation angle is given by;

$$\int_0^{\gamma} v_{pk} \sin(\omega t)\, \mathrm{d}(\omega \mathrm{t}) = \int_{I_{dc}}^{0} (-2L_c\omega)\, \mathrm{di}_1(\mathrm{t}) \tag{3.9}$$

giving;

$$\gamma = \cos^{-1}\left(1 - \frac{2L_c\omega I_{dc}}{v_{pk}}\right) \tag{3.10}$$

The analysis is simplistic as the effects of commutator device voltage drops and machine phase resistances are neglected. Nevertheless, this is reasonable because the phase voltage, commutating inductance and level of dc current being commutated are by far the dominant parameters.

Measured commutator phase currents of two adjacent commutator phases during current commutation are shown in figure 3.12.

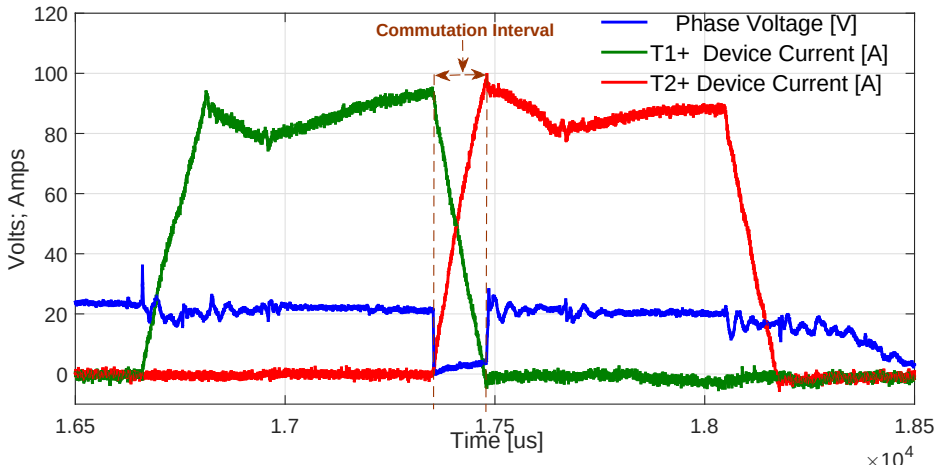

Fig. 3.12 Measured Commutator Phase Current Commutation Waveforms

Figure 3.13 shows the simulated waveforms for a 24 phase machine operating in the generating quadrant showing the machine phase voltage, commutator phase current, machine phase current and dc link voltage & current waveforms. For an even number of stator phases assuming a constant dc link current, the phase winding current is a rectangular waveform and the phase rms current is given by;

$$I_{rms} = \frac{I_{dc}}{2} \tag{3.11}$$

If the device voltage drops and commutation overlap γ are neglected, the dc link voltage can be easily calculated by integrating the coil voltages outside the

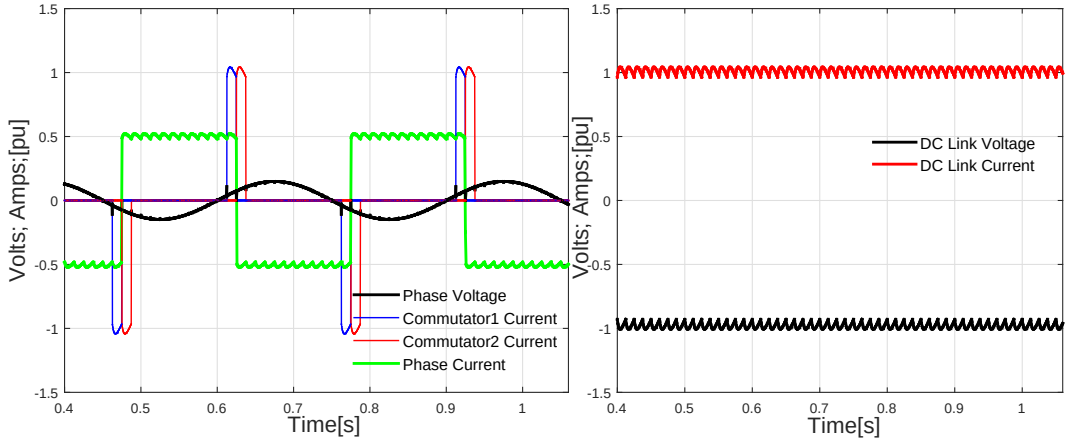

Fig. 3.13 Simulated 24 Phase Machine Phase Voltage, Commutator Phase Current, Phase Current, DC Link Voltage & Current for Generator Mode of Operation

commutation zone to give;

$$V_{dc} = \frac{\sqrt{2}}{\pi} N v_{ph} \cos\alpha \tag{3.12}$$

where; v_{ph} is the rms phase voltage, α is the commutator firing angle and N is the number of machine phases.

It is clear from the above analysis that, for a given machine stator frequency ω, the commutation interval increases with L_c & I_{dc} and decreases with increasing phase voltage v_{pk} behind the commutating inductance. Equation 3.10 highlights two key fundamental machine design parameters that can be optimised to give desired electronic commutator performance. Firstly, it highlighted the dependence of the commutation interval on the machine peak phase voltage available during commutation and, secondly, the dominant effect of machine phase commutating inductance on the current commutation process. These two factors will be briefly examined in more detail in the following paragraphs.

3.3.4 Influence of Peak Phase Voltage (V_{pk}) on Current Commutation

It is clear from (3.10) that the commutation interval is influenced by the amplitude of the available voltage behind the commutating reactance of the respective phase undergoing commutation. In order to maximize machine torque output, it is desirable to minimize the commutation interval γ. To achieve this, commutating poles or

interpoles are employed in conventional dc machines to guarantee a voltage sufficient enough to counter the reaction voltage that is induced in the commutating coil as per Lenz's Law. Some work reported in [88] attempted to replace the commutating poles by providing the necessary commutating emfs from external electronic circuits. However, the proposal was thwarted by the fact that the machine topology was not capable of full four quadrant operation and still suffered from some of the mechanical commutator drawbacks since brushed commutation was still employed.

Equation 3.10 highlights that by maximising the voltage available for commutation at the end of the outgoing conduction period and the start of the commutation, the commutation interval γ can be reduced. However, this observation goes against conventional sinusoidal back emf machine designs since the voltage naturally approaches zero at near the machine q-axis (geometric neural position) where phase current commutation is desirable to maximize machine torque output. Furthermore, owing to the swapping of the armature and rotor circuit in this fully electronically commutated topology, commutating poles can not be easily realised as the field circuit is now on the rotating part of the machine, bearing in mind that the overall goal is to replace all mechanical brush arrangement with electronic means.

If however, the machine airgap flux waveform is modified to give a near trapezoidal waveform as opposed to sinusoidal waveform, the peak phase voltage available to aid stator current commutation can be maximised, leading to a consequent reduction in commutation interval. The disadvantage of this approach is that trapezoidal airgap flux and back emf has a significant proportion of low order harmonics that can adversely affect the machine performance. However, having alluded to the diminished impact of low order harmonics on multiphase machines if the phase number is sufficiently increased, the adverse effects of low order harmonics on machine performance are significantly curtailed and can be considered negligible if the phase number is sufficiently increased. Instead, if the stator phase number is sufficiently increased, the low order harmonics are beneficially exploited to maximize machine torque density [37],[40], [42],[89]. It is therefore desirable to design the machines of this topology with trapezoidal airgap flux distribution to maximize the phase voltage available to assist current commutation. Trapezoidal airgap flux waveform brings other additional benefits such as increased machine torque density for a given stator volume com-

pared to sinusoidal airgap flux designs. One of the experimental prototype drives was specifically designed to give trapezoidal airgap flux and the experimental validation work discussed in later chapters will expose some of the desirable attributes of this trapezoidal machine airgap flux approach. The results from this experimental drive has shown that despite the best efforts to increase the commutation voltage by using trapezoidal airgap flux, armature reaction has a far dominant undesirable effect which tends to reduce the phase voltage available at the commutation interval, particularly at high per unit armature currents. Figure 3.14 shows experimental measurement of commutator phase current and corresponding machine phase voltage, highlighting the phase voltage reduction due to armature reaction. Nevertheless, compared to sinusoidal airgap flux designs, trapezoidal flux designs still result in higher phase voltage at the commutation interval and also facilitates beneficial exploitation of lower order space harmonics to maximize torque density.

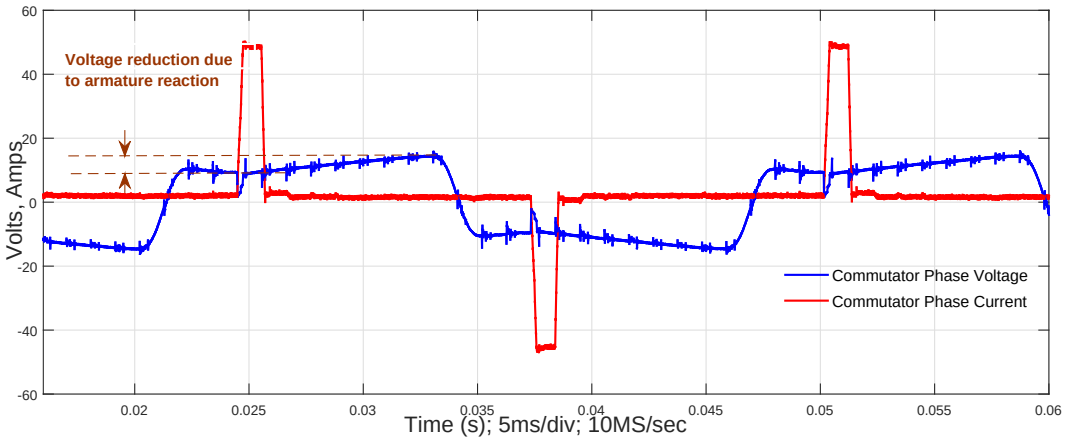

Fig. 3.14 Armature Reaction Effects on Phase Commutation Voltage

3.3.5 Influence of Commutating Inductance (L_c) on Current Commutation

The electronic commutator's phase current commutation interval is also influenced by the machine phase commutating inductance as highlighted in (3.10). Before highlighting the impact of commutating inductance, a brief definition of the machine commutating inductance is given here.

During the commutation process as described in the preceding analysis, the transient current flow in the machine phase undergoing commutation gives rises to a changing flux linkage in the coil(s) undergoing commutation. A reaction voltage is induced, as per Lenz's law, opposing the flux change, and is of the form $L_c\frac{di}{dt}$. The L_c component is the commutating inductance, and in essence is a measure of the change in flux linkage with respect to a change of current. The induced reaction voltage due to current reversal in the commutating coil acts to oppose any change in current and thus delays commutation. For example, induced voltage in phase 1 e_1 can be expressed as;

$$e_1 = -(L_c\frac{di_1}{dt} + \sum_n M_{1-n}\frac{di_n}{dt}) \tag{3.13}$$

Where i_1 is the phase 1 current, i_n is the n^{th} machine phase, M_{1-n} is the mutual coupling between phase 1 and phase n, L_c is the phase commutating inductance, n is the number of machine phases that have mutual coupling with phase 1.

The commutating inductance is closely related to the steady state coil inductance, and is made up of components that see a net change of flux linkage during commutation. As the current commutates in a coil side situated in a slot, the cross slot leakage flux must also change. This change in flux linkage contributes to the commutating reaction voltage. In the case of machines with uniform damper windings the flux path is predominantly in air and not subject to saturation, as such, there is a linear relationship between change of flux linkage and change of current. Therefore, the inductance must be the same as the steady state cross slot leakage inductance component. The mutual component of cross slot leakage also contributes to the reaction voltage as expressed in (3.13). The commutating inductance can be expressed as:

$$L_c = L_{slot} + L_{end} \tag{3.14}$$

where L_{slot} is the slot leakage inductance and L_{end} is the end winding inductance of the two overhangs of a phase winding. The slot and end winding inductances can be calculated in the conventional manner as given in [90], [91], [35] and will not be repeated here. These inductance components relate to undesirable leakage paths that do not contribute any useful flux into the air gap (where torque is produced) but have a direct impact on the design and operation of the electronic commutator due to their

influence on the commutating reaction voltage. Its worth bearing in mind that the airgap inductance is not included in the commutating inductance because the reducing current in the coil undergoing commutation is matched by a current rising at the same rate in another coil, such that the armature reaction flux does not vary appreciably and therefore does not generate any reactance voltage. In other words, the commutation of a coil is linked to the immediate commutation of the next coil, so any main pole axis flux component has the same value at the beginning and end of the commutation, therefore can not cause other than zero average induced voltage in the commutating coil [76]. The commutating inductance is thus, the effective inductance of a circuit

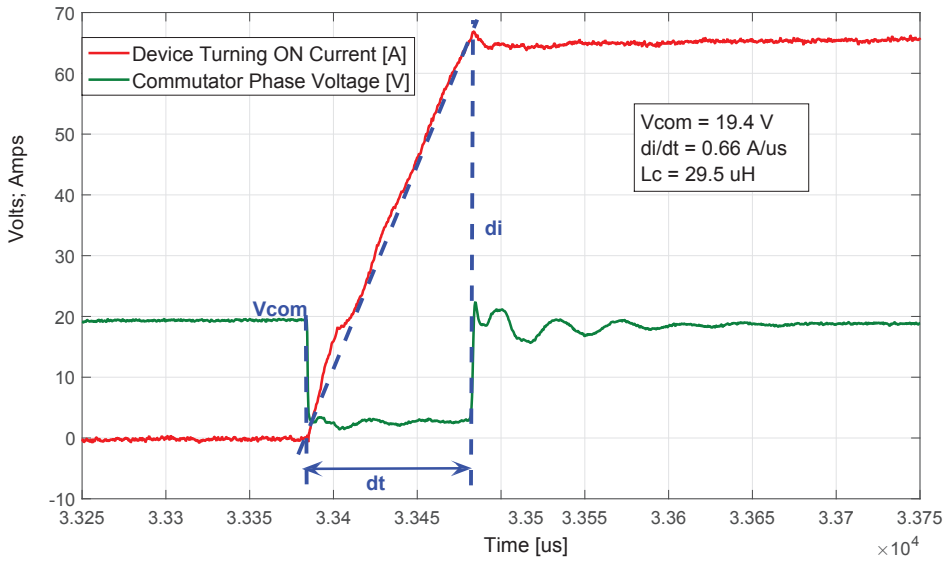

Fig. 3.15 Commutating Inductance Measurement on 24 phase Prototype Machine

between two adjacent commutator segments. In other words, its the ratio between the rate of change of current in the commutating coil and the voltage that is causing the rate of change. This is illustrated in Figure 3.15 which shows the calculated commutating inductance from the experimental measurement.

Effects of Commutating Inductance on Electronic Current Commutation

The commutating inductance has a direct impact on the design and operation of the electronic commutator. From an electronic commutator power electronics design viewpoint, a very low commutating inductance is desirable for the following reasons.

Firstly, the magnetic energy stored in the commutating inductance ($\frac{1}{2}L_cI^2$) of the machine and the reaction voltage developed during current commutation has to be addressed and accounted for in the electronic commutator power electronic circuit design. It is clear that snubber circuits or capacitive clamp circuits will be required to store this energy and arrest the associated over-voltages to within the safe operating area of the semiconductor devices. It therefore follows that higher commutating inductance will require bigger snubber / clamp circuit components and semiconductor devices with increased voltage rating, resulting in less compact & costly commutator designs.

Secondly, the energy transferred to the snubber or clamp circuits has to be either resistively dissipated as heat thereby adversely impacting drive efficiency and also posing thermal management challenges. Alternatively, the energy has to be recovered by use of additional energy recovery circuits.

Thirdly, higher commutating inductance results in bigger commutation notches for a given current which curtails regulation of output DC voltage when machine is operated as a generator. Therefore, the machine commutating inductance must be kept as low as is practicable to facilitate electronic commutator design. The ultimate motivation of this work is to produce a machine with an integrated power electronic converter as one unit. As such, the machine and power electronics design must be carried out simultaneously to produce an integrated drive unit.

The disadvantage of the lower commutating inductance approach is that the machine prospective fault currents increase with the reduction in the commutating inductance, which has a direct adverse impact on the current rating of the electronic commutator devices. As such, a compromise has to be reached at the design stage between desired peak fault currents and electronic commutator circuit peak current rating.

The next section extends the analysis to the topology with an odd number of stator phases. This will then be followed by a comparative analysis of the key performance advantages and disadvantages of these two topologies.

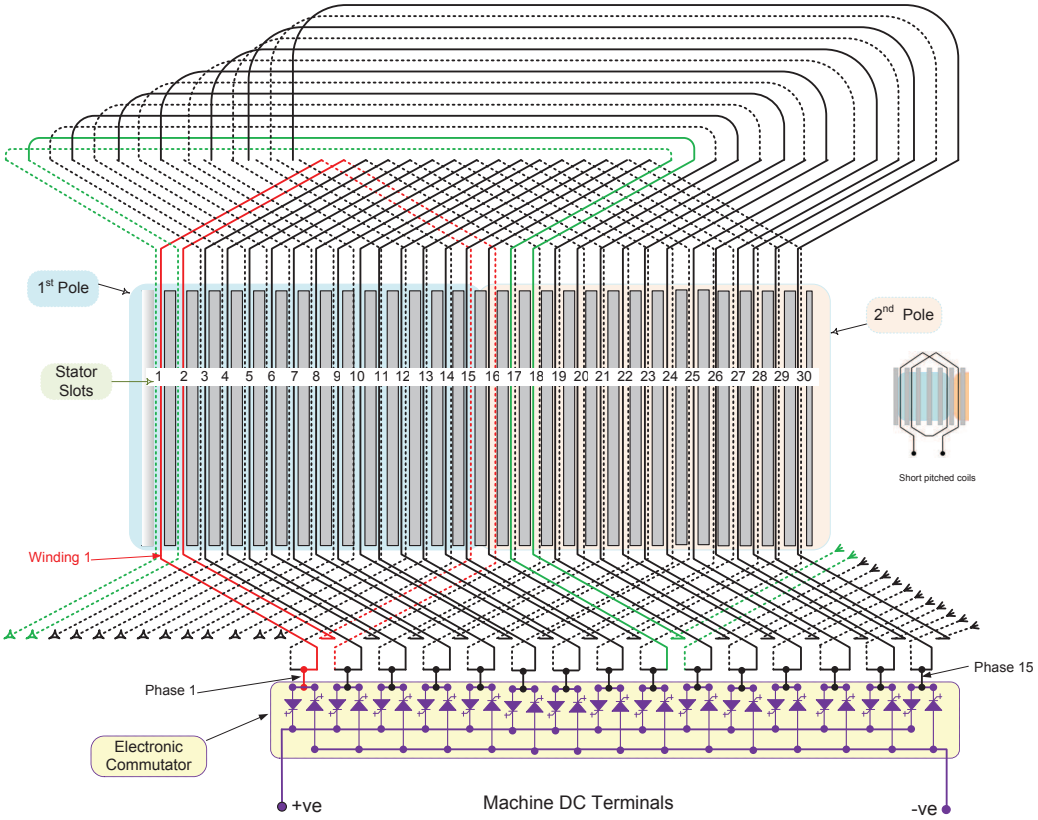

Fig. 3.16 A 15 Phase Machine with 30 stator slots, 2 Rotor Poles and Simplified Electronic Commutator

3.4 Odd Stator Phase Number

This topology features a plurality of stator phases connected to form a polygonal machine winding with N stator phases, where N is an odd number. All the stator phase winding functions are phase displaced equally by $\frac{2\pi}{N}$ radians (electrical) and connected to form a complete polygonal winding similar to the even number topology. For example, figure 3.16 depicts a machine with fifteen stator phase windings, each comprising of two single coils connected in series, two rotor poles and its simplified electronic commutator circuit. Analysis of this topology has shown that owing to the odd number of stator phases, simple fully pitched stator phase windings cannot be employed as this would result in net circulating currents in the polygon during machine operation due to the phase voltage imbalances on the two current paths of the stator polygon. The analysis has revealed that to prevent a net circulating current in the polygon, the machine winding function must be designed such that the induced phase voltages (machine back emf) do not contain the N^{th} voltage harmonic. In fact,

simulation studies have shown that the presents of the N^{th} voltage harmonic will drive a net circulating current in the machine stator polygonal winding. Elimination of the N^{th} voltage harmonic component can be readily achieved by employing short pitching and connecting the short pitched coils in series such that the resultant phase winding function does not have any N^{th} voltage harmonics. This has been experimentally validated on a prototype machine as will be highlighted later in the experimental work.

3.4.1 Theory of Operation

In general, most of the fundamental operating principles of this topology are similar to that of the even numbered topology, therefore only the specific differences will be highlighted here. An analysis of the possible commutation control strategies for the odd numbered topology has shown that unlike the case with even number of stator phases, the simultaneous current commutation of the two diagonally opposite phases is no longer permissible due to the non symmetric nature of the phase number. In fact, simulation study has shown that adopting the same symmetric commutator control strategy developed for the even number topology results in significant net circulating currents in the machine stator polygonal winding.

An alternative asymmetric electronic commutator control strategy has been developed and validated via simulation and on an experimental prototype drive. This scheme employs a form of interleaved electronic commutator phase device switching strategy. This can be illustrated using the 15 phase machine topology depicted in figure 3.16. When the device connecting phase 1 machine winding to the dc positive rail is undergoing commutation, the devices connecting $(\frac{N}{2} \pm 1)$ machine winding phases to the negative dc rail can not be simultaneously undergoing commutation. In-fact, the corresponding device $(\frac{N}{2} \pm 1)$ to undergo commutation on the negative dc rail must be phase displaced by $(\frac{\pi}{N})$ radians from the commutating device on the positive dc rail. Thus, when phase 1 device connected to positive dc rail undergoes commutation at rotor position angle θ, phase 7 and phase 8 devices connected to the negative dc rail will undergo commutations at $(\theta - \frac{\pi}{N})$ and $(\theta + \frac{\pi}{N})$ radians respectively, for positive rotational direction of the rotor. In other words, the sequential commutations of all the phase winding devices that connect the phase windings to the positive dc rail are phase

displaced by ($\frac{\pi}{N}$) radians relative to the sequential commutations of the devices that connect the phase windings to the negative dc rail, i.e. they are interleaved. Figure 3.17 shows simulated waveforms from a 15 phase topology, the top plot shows the interleaved top and bottom commutator phase devices that are turned ON. The bottom figure shows the corresponding machine voltages and currents waveforms.

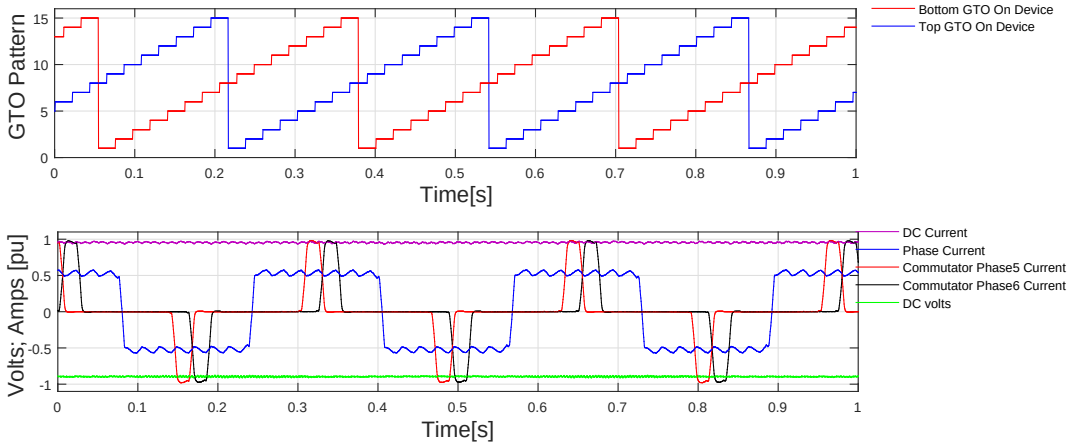

Fig. 3.17 Simulated Waveforms of a 15 Phase Machine in Generating Mode

3.4.2 Current Commutation In Odd Numbered Topology

Owing to the asymmetric operation due to odd number of stator phases, the electronic commutator operating states are different from those of even numbered machines depicted in figure 3.8.

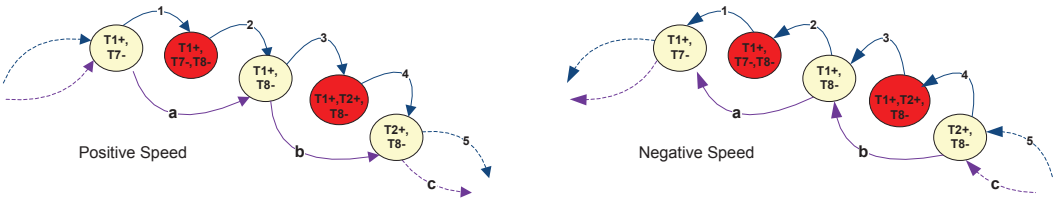

Fig. 3.18 Odd Phase Number Commutator State Machine

For the odd number of stator phase topology, interleaved electronic commutator switching strategy has been implemented and shown to give the desired electronic commutator operation and effectively suppresses circulating currents in the machine stator polygonal winding. The interleaved strategy illustrated by the state machine of figure 3.18 was implemented and practically shown to give desired operational behaviour.

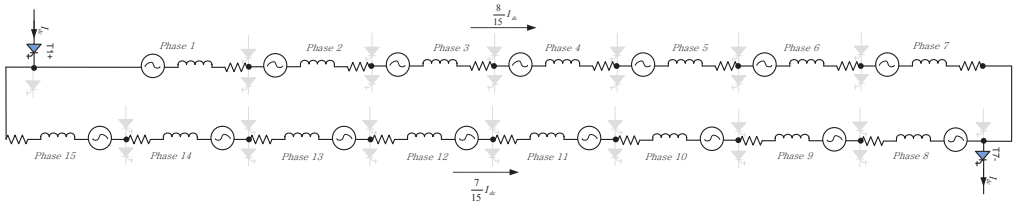

Fig. 3.19 15 Phase Machine Circuit Diagram before First Commutation

Similar to the state machine of even numbered topology, both direct state transitions and indirect state transitions through intermediate commutation states shown in shaded area (red) are equally applicable. A circuit representation of the operation is depicted in figure 3.19 which shows the equivalent circuit current paths when phase 1&7 commutator segments are injecting current into the machine stator. The next phase to undergo commutation will be phase 7 by transferring current to phase 8 commutator segment. Figure 3.20 shows the machine stator circuit after current commutation to stator commutator phase 8 segment, now phase 1 & 8 commutator segments are injecting current into machine stator. The next phase to undergo commutation will be phase 1 by transferring current to phase 2 commutator segment. Figure 3.21 shows the machine stator circuit after current commutation to stator commutator 2 segment, now segments 2 & 8 are injecting current into machine stator. By analysing the basic circuit current relationships, the winding phase current at any instant in time can be expressed as;

$$i_w(t) = \frac{I_{dc}(t)}{2}\{1 - f(n(t))(\frac{1}{N})\} \tag{3.15}$$

$$f(n(t)) = \begin{cases} 0 & \text{if } n \text{ is even} \\ 1 & \text{if } n \text{ is odd} \end{cases}$$

where; n is the number of stator phases in series on the respective half section of machine polygonal winding. The function *f(n(t))* represents an interleaving modulating control function for the electronic commutator devices that dictates the number of seriesed phases on each half of the machine polygon at any given instant.

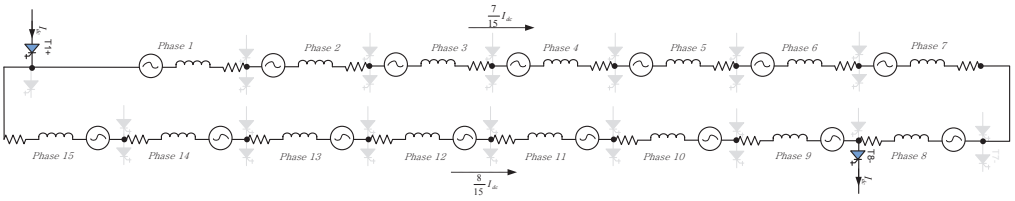

Fig. 3.20 15 Phase Machine Circuit Diagram After First Commutation

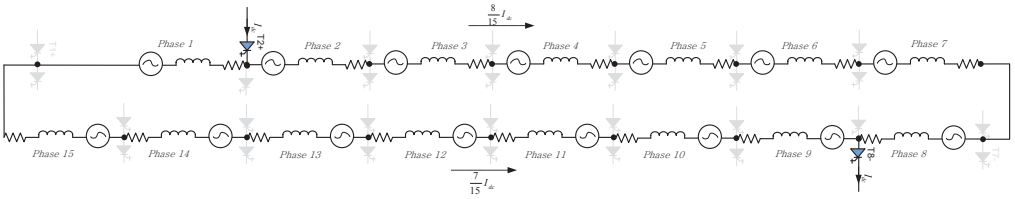

Fig. 3.21 15 Phase Machine Circuit Diagram After Second Commutation

3.4.3 Electronic Commutator Current Commutation Analysis

The phase current electronic commutator analysis and factors affecting electronic current commutation presented in section 3.3.3 for the even numbered topology also hold for the odd numbered topology, as such the analysis will not be repeated here. The key notable difference is the interleaved commutator phase device switching strategy required for odd numbered topology. The interleaving switching function *f(n(t))* given in (3.15) is synchronised to the stator phase voltage vector and is defined such that each commutator phase device conducts current for an interval (in radians) given by;

$$\varepsilon = 2\frac{\pi}{N} \pm \mu \tag{3.16}$$

where, N is odd and denotes the number of stator phases, μ is the overlap angle that defines the indirect commutation transition interval highlighted in figure 3.18 when two adjacent commutator segments are both conducting phase current. Figure 3.22 shows the simulated waveforms for a 15 phase machine operating in the generating quadrant. The effects of the interleaving switching function can be clearly seen on the machine phase current waveform as a modulating function whose frequency is N times the machine fundamental frequency. A closer analysis of the effect of the modulation function reveals that this modulating function eliminates the N^{th} harmonic from the phase current waveform. An FFT of the phase current given in figure 3.23 clearly shows the absence of the 15^{th} harmonic current component for the simulated 15 phase

machine which would have lead to a net circulating component in the machine stator polygon. It is also clear from figure 3.22 that the proposed control strategy results in no circulating current in the machine polygonal winding. By taking the square root

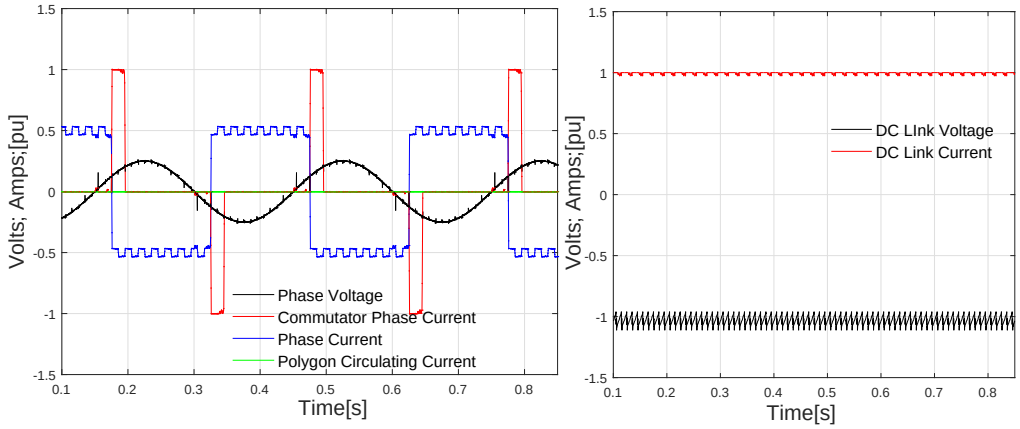

Fig. 3.22 Simulated 15 Phase Machine Phase Voltage, Commutator Phase Current, Phase Current, DC Link Voltage & Current for Generator Mode of Operation

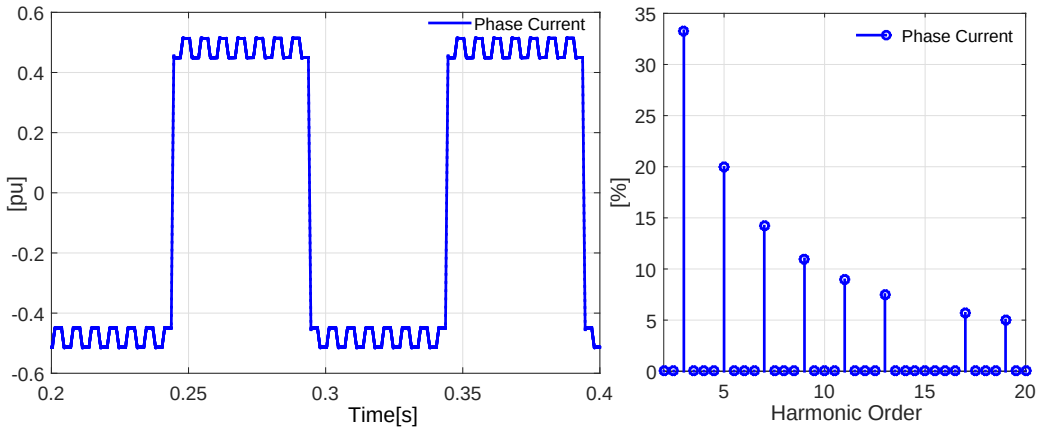

Fig. 3.23 15 Phase Machine Phase Current & Phase Current FFT Plots

of the arithmetic mean of the squares of the values of the phase current waveform, its rms value can be represented as;

$$I_{rms} = \frac{I_{dc}}{2}\sqrt{1-(1/N)^2} \tag{3.17}$$

where, I_{dc} is the machine output dc link current and N is odd and defines the number of stator phases. Its clear from (3.17) that for a given dc link current and number of stator phases, the odd number topology gives a lower machine phase rms current

despite having the same peak value as the even number topology. Figure 3.24 and 3.25 show measured waveforms from the 15 phase experimental prototype machine showing the two adjacent commutator device currents, machine phase voltage and current waveforms in generating mode when operated in natural commutation and hybrid commutation modes respectively. Frequency domain examination of the phase current waveform also confirmed the absence of the 15th current harmonic component, which agrees with the simulation.

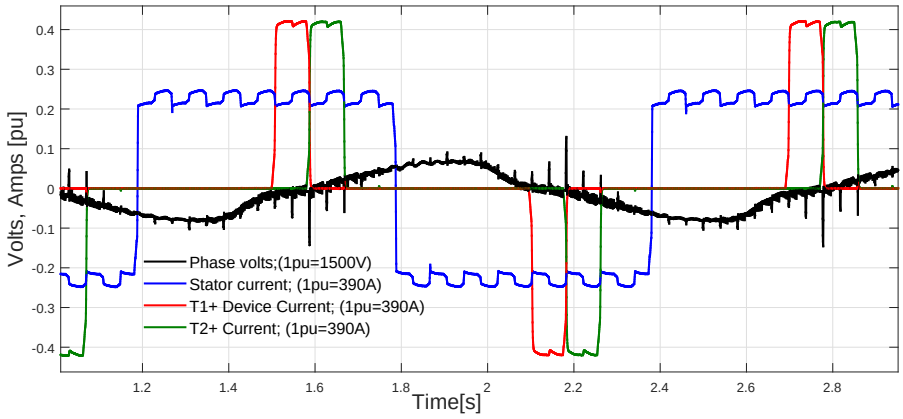

Fig. 3.24 Experimental 15 Phase Machine Measured Waveforms in Generator Mode of Operation with Natural Current Commutation

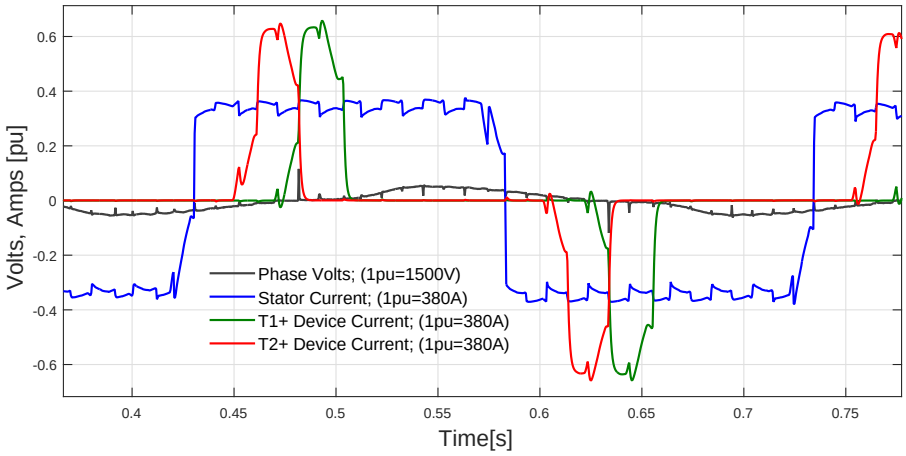

Fig. 3.25 Experimental 15 Phase Machine Measured Waveforms in Generator Mode of Operation with Hybrid Current Commutation

Simulation and experimental results of a 15 phase machine under normal operating conditions over the entire machine torque/speed range have confirmed that the proposed interleaved commutator control strategy results in no net circulating current in the

machine stator polygonal winding, which was the main concern of the odd number topology.

Having presented the working principles and highlighting some of the operational attributes of both even and odd number topologies, a comparative analysis of the two topologies will now be discussed. However, before embarking on this analysis, its important to first highlight some of key practical implementation aspects of the electronic commutator power electronic circuits common to both even and odd number topologies that had to be addressed. These implementation aspects have a direct impact on the design and operational characteristics of these two topologies, as such, they feed into the comparative analysis that follows.

3.5 Practical Implementation Aspects of Electronic Commutators

The electronic commutator circuitry highlighted so far has been simplified to aid clarity. However, for practical implementation of the power electronic commutator circuit, additional circuitry will be required to ensure correct and safe electronic current commutation to avoid compromising the switching devices safe operating area. The analysis, modelling and experimental work has shown that these additional auxiliary circuit requirements differ depending on whether the even or odd number topology is chosen. In order to highlight these practical aspects, a generic practical commutator circuit operating principle will be described before the topology comparative analysis.

3.5.1 Practical Commutators: Current Commutation Process

The circuit depicted in figure 3.26 will be used to describe the current commutation between two adjacent machine stator phases of the electronic commutator. The circuit depicted in this figure consists of two electronic commutator phases 1 & 2 switching devices, T_1, T_2 and T_3, T_4 respectively and additional auxiliary commutation circuits comprising of diodes D_1, D_2 and D_3, D_4 connecting the machine phase 1 & 2 windings to the dc link poles through clamp capacitors C_+ and C_- which form an auxiliary dc

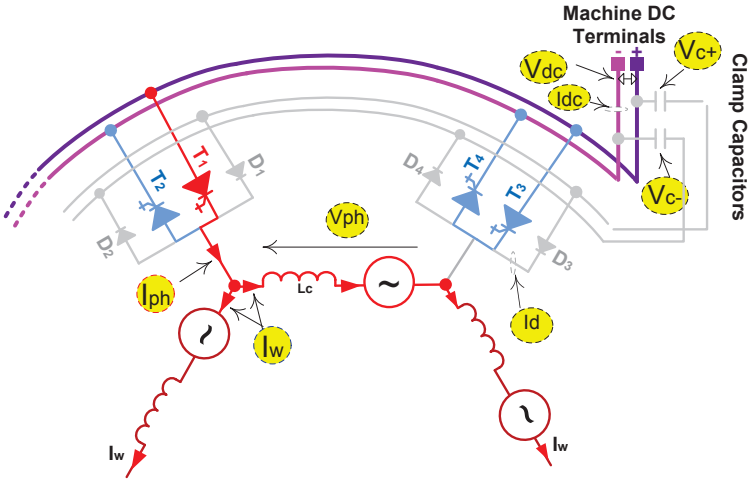

Fig. 3.26 Two Level Machine & Converter: Showing Only Two Electronic Commutator Segments and Their Machine Phase Connections

rail. The following signal definitions are used in the following current commutation stages description.

V_{dc}: This is the voltage across the machine output dc terminals;

I_{dc}: This is the machine output dc link current;

V_{ph}: This is the voltage across the phase winding given by;

$$V_{ph} = E_{emf} + I_{ph}R + L\frac{dI_{ph}}{dt}. \tag{3.18}$$

where; E_{emf} is the induced machine back emf, R & L are the machine phase resistance and inductance. The firing of the electronic commutator devices is synchronised to this voltage.

I_{ph}: This is the current pulse that is conducted by the electronic commutator phase leg devices connecting the machine phase winding to the dc link. Its peak amplitude is equal to the dc link current, however the current pulse duration is only $\frac{2\pi}{N}$ of the fundamental cycle, where N is the number of stator phases.

I_w: This is the current in the machine phase winding. Its peak value is half that of the dc link current owing to the two parallel paths formed by the commutator devices connecting the machine polygonal winding to the dc terminals.

It is assumed that power electronic switching devices T_1 and T_2 sequentially connects the machine phase 1 winding to the positive and negative dc poles respectively. Similarly T_3 and T_4 sequentially connects the machine phase 2 winding to the positive and negative dc poles respectively. All machine phases have similar auxiliary clamp diode circuits that connect to the same clamp capacitors C_+ and C_-. The Clamp voltages ($V_{c\pm}$) shown in figure 3.26 are the voltages developed across the auxiliary voltage clamping capacitors when the clamping diodes conduct current to arrest over voltages across the commutating devices. For reasons of clarity, only current commutation from phase 1 to phase 2 will be described. However, it should be borne in mind that similar commutation process will be occurring on the respective machine commutator phase segments that connect to the negative dc pole to complete the machine current path.

The electronic commutator power electronic switching devices switch at the machine fundamental frequencies which tend to be inherently very low. Its envisaged that machine fundamental frequencies will be typically less than 200Hz, which is very low in comparison to the pulse width modulated device switching frequencies which are typically in the range of 1kHz to 20kHz. This low switching frequency means power electronic devices can be optimised for low conduction losses, since switching losses are almost negligible. This feature can be exploited in the power electronic switching modules design to yield compact and very high converter efficiencies. Additionally, the undesirable electromagnetic interference effects of high $\frac{dv}{dt}$ and high $\frac{di}{dt}$ associated with high PWM frequencies are significantly curtailed by the low switching frequencies used in this machine/converter topology.

Current Commutation Stages

The current commutation stages described here apply to both even and odd numbered topologies. Simulated waveforms of a 24 phase machine electronic commutator will

be used to illustrate the working principle. In this case *under-commutation*, similar to conventional dc machines where the brush-gear moves to the next commutator segment before the current has reached zero in the outgoing commutator segment is highlighted. The electronic commutator states during phase current commutation are depicted in the figures 3.27 to figure 3.30.

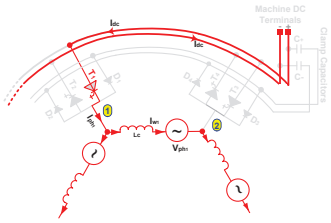

Fig. 3.27 Commutator Currents Path Before Start of Commutation

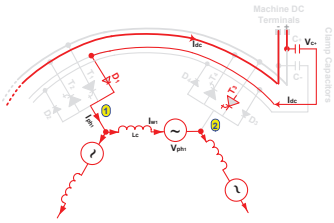

Fig. 3.28 Commutator Current Diverted to Clamp Circuit

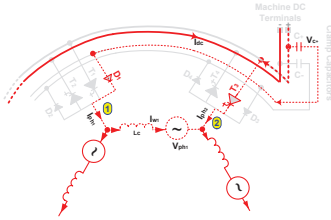

Fig. 3.29 Commutator Currents Transfer to Device T_3

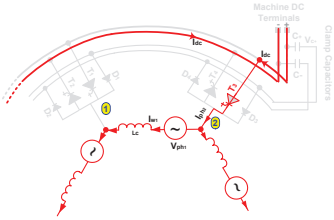

Fig. 3.30 Commutator Current fully Commutated to T_3

Stage 1: Before Commutation Starts

It will be assumed that before phase current commutation starts, the dc link current is being injected into the machine through device T_1 on phase 1 of the commutator as highlighted in figure 3.27, i.e. period before *t=1.185s* in figure 3.31 & figure 3.32. The device T_2 which connects the machine phase 1 winding to negative dc rail is off (not gated) and the current returns to the negative dc terminal through a similar device on the phase which is symmetrically opposite as alluded to earlier, in this case phase 13 for a 24 phase machine. Before phase 1 current commutation starts, the phase 1 winding current polarity is such that current flow is from phase 1 to phase 2 winding. When phase 1 current commutation is complete, its phase winding current will have reversed polarity to current flow from phase 2 towards phase 1.

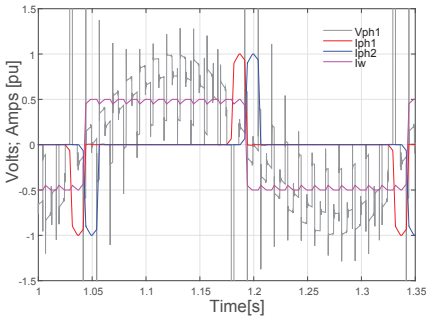

Fig. 3.31 Simulated Machine Phase currents for a 24 Phase Machine

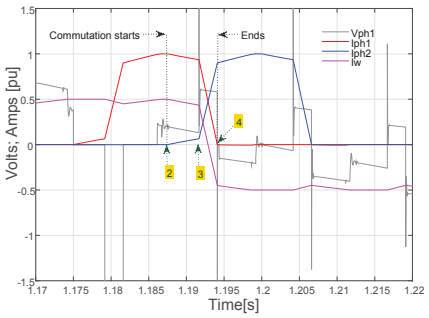

Fig. 3.32 Zoom of figure 3.31 showing Current Commutation Stages

Stage 2: T_3 Turned ON

This stage starts when device T_3 is turned ON, assuming there is some degree of overlap (μ) between turning T_3 ON and turning T_1 OFF. This is the period highlighted with an arrow 2 in figure 3.32 and figure 3.34. The current will start to commutate from T_1 to T_3 at a slow rate owing to the low reactance voltage e. The commutation duration t_c is given by:

$$t_c = \frac{e}{2.I_w.L_c} \tag{3.19}$$

Its worth noting at this stage that the current commutation between T_1 and T_3 can be forced to occur rapidly by force commutating device T_1 or naturally if sufficient overlap (μ) is inserted between turning ON the incoming device and turning OFF the outgoing device. The overlap angle is an additional parameter that can be exploited to optimise the electronic commutation process.

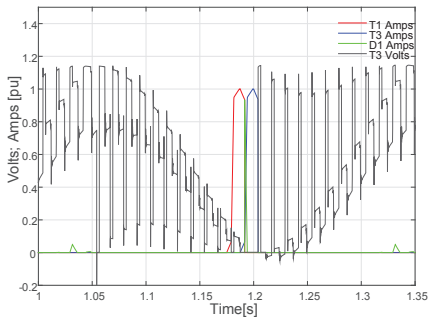

Fig. 3.33 T_1, T_3 Currents & T_3 Volts for a Fundamental Cycle

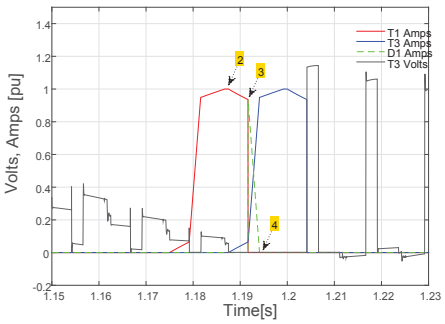

Fig. 3.34 Zoom of figure 3.33 showing Current Commutation to D_1

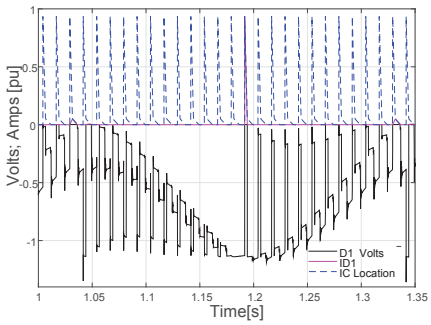

Fig. 3.35 Diode D_1 Volts & Amps and Clamp Circuit Current

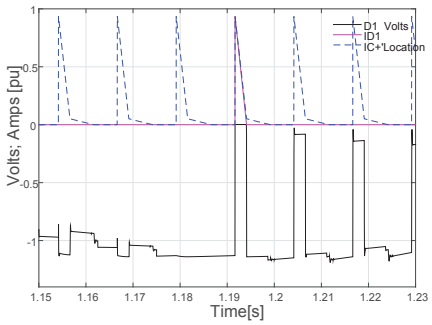

Fig. 3.36 Zoom of figure 3.35 showing Current Commutation to D_1

Stage 3: T_1 Turned OFF

This stage is marked as state 3 in figure 3.32 and figure 3.34 and starts when device T_1 is gated OFF. When the device T_1 is force commutated, a reaction voltage is induced in phase 1 winding, as per Lenz's law, due to the presence of the commutating inductance L_c opposing the flux change. This voltage polarity is such that the incoming device T_3 is reverse biased and thus can not instantaneously conduct all the phase current. Instead, the induced voltage forward biases the clamp circuit diode D_1 as shown in figure 3.35 & figure 3.36 at *t=1.192s*. Consequently, the phase current commutates from T_1 to D_1 through the positive clamp capacitor C_+ as depicted in figure 3.28 and rapidly builds up at a rate determined by the stray inductance in this auxiliary circuit loop. This rapidly charges the clamp capacitor to a voltage V_{C+}. Eventually the sum of the phase 1 voltage and clamp capacitor voltage becomes positive and sufficiently large ($V_{ph1} + V_{C+} > 0$) to initiate rapid current commutation from phase 1 clamp diode D_1 to the incoming device T_3. At this stage, the machine phase 1 winding is effectively short circuited as shown in figure 3.29. The current progressively transfers from D_1 to T_3 at the same rate, where the sum of the two currents equal the dc link current i.e. ($I_{D1} + I_{T3} = I_{dc}$). The phase 1 winding current reaches zero when the current through diode D_1 equals that going through the incoming device T_3 i.e. $I_{w1} = 0$ at $I_{D1} = I_{T3}$. After this point the phase 1 winding current reverses polarity and starts rising in the opposite direction.

Stage 4: D1 Turns OFF

The current in D_1 continues to transfer to the phase 2 commutator device T_3 until it eventually fully commutates from D_1. At this point, D_1 current reaches zero and it stops conducting current and no more current flows through the auxiliary clamp capacitor C_+, all the dc current is now in the main dc rail and at this stage the winding phase current has fully reversed polarity. The commutation is completed when diode D_1 stops conducting and turns off and all the current is through T_3 as depicted in figure 3.30. A similar process is repeated 180 degrees (electrical) later, on the same phase 1 and phase 2 but this time the device undergoing commutation will be those that connects to the negative rails of the main and auxiliary dc rails i.e. T_2, D_2, T_4 and D_4.

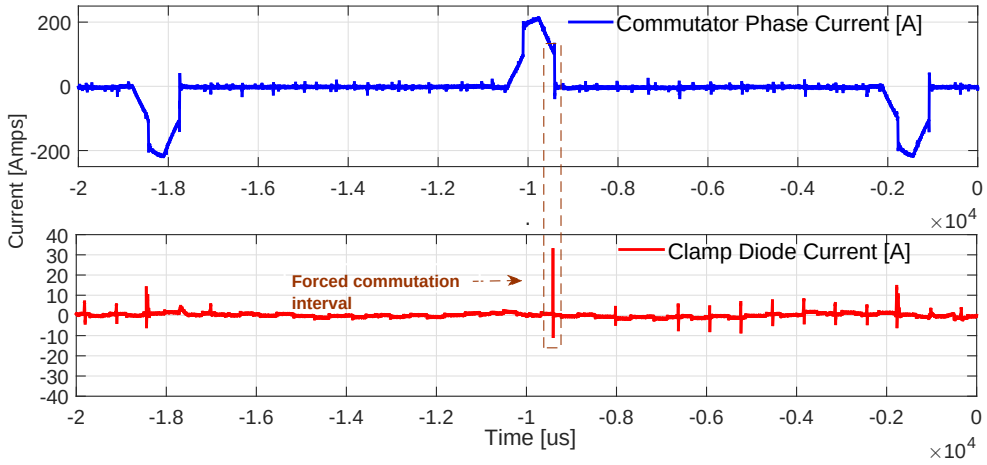

Fig. 3.37 Commutator Phase Current Commutation Through Clamp Diode

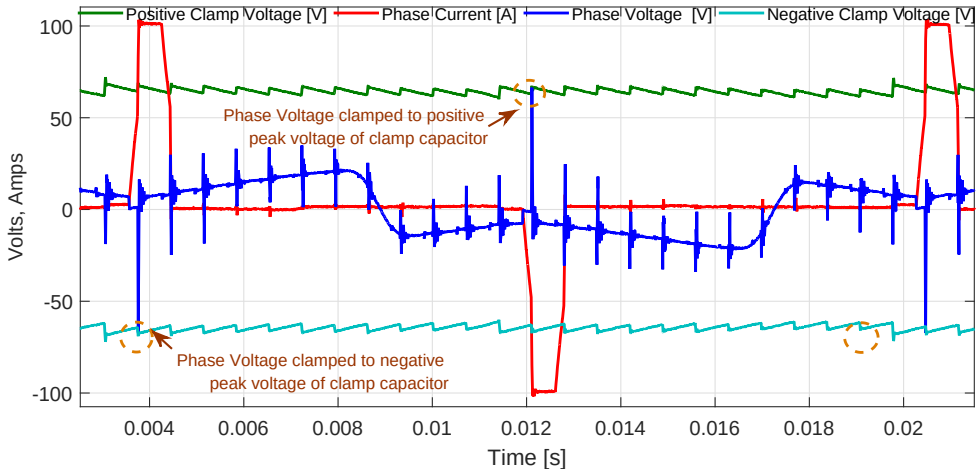

Fig. 3.38 Commutator Phase Current Commutation Through Clamp Diode

Figure 3.37 and figure 3.38 shows the measured waveforms from the 24 phase experimental prototype drive highlighting current commutation over a fundamental cycle. The auxiliary clamp diode conduction periods can be clearly seen during current commutation intervals as highlighted in figure 3.37. Owing to the strong mutual coupling between adjacent machine phases, additional pulses of diode current can be seen coinciding with the commutation events in the respective adjacent phases. Figure 3.38 shows the measured phase current, phase voltage and the two auxiliary clamp capacitor voltages over a fundamental cycle. It can be seen that the machine phase voltage is effectively clamped to the auxiliary clamp capacitor voltage amplitude during phase current commutation. The spikes on the phase voltage waveform coincide with the machine phase current commutation events.

3.6 Electronic Current Commutation Modes

The electronic commutator control schemes highlighted earlier introduced the concept of direct and indirect commutation state transitions. The modelling and experimental work has demonstrated that the current commutation process in these electronically commutated machine topologies can be controlled to occur in three distinct commutation modes namely; (a) natural commutation, (b) forced commutation and (c) hybrid commutation all governed by controlling the transition states between current commutation. Each of these commutation modes is also influenced by the choice of power electronic switching devices used, the overlap angle μ applied between the switching devices being turned OFF and that being turned ON and the reaction voltage and machine commutating inductance. Figure 3.39 shows the equivalent circuit for adjacent phases and the corresponding current path during transitions.

1. **Natural Commutation**: The commutation is deemed natural when the turning-on of the in-going commutator device leads to the turning-off of the out-going phase commutator device without the need of turn-off gating signals of the out going devices. The current commutation is via an intermediate state as highlighted earlier in figure 3.8. In this mode simple diode and Thyristor devices can be employed if only natural commutation is required for the specific

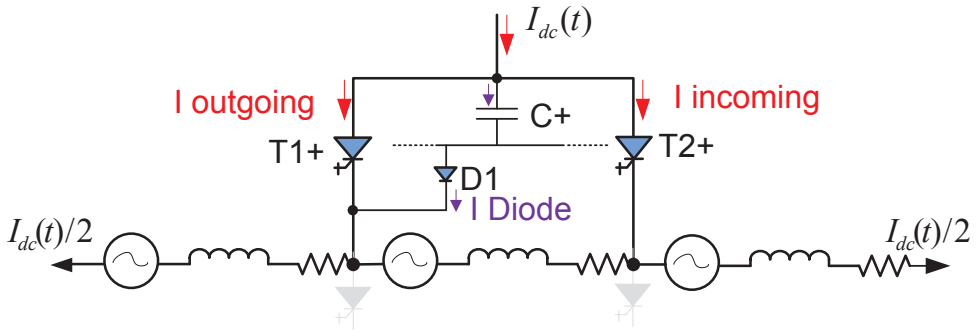

Fig. 3.39 Schematic showing current paths

application. Figure 3.40 shows measured current waveforms for natural current commutation between adjacent machine commutator phases. It can be seen in this figure that the clamp diode D_1 hardly conducts any current during natural commutation, as such the clamping circuitry is not required for this commutation mode.

Natural commutation operation can result in reduced output power of the drive if the machine commutating inductance is significant as this results in volts seconds loss due to large commutation overlap angles. A benefit of natural commutation is that simple Thryistor devices can be used with simple commutation auxiliary voltage clamping circuits owing to the fact that there will be little energy transfer to the auxiliary commutation circuits during natural commutation.

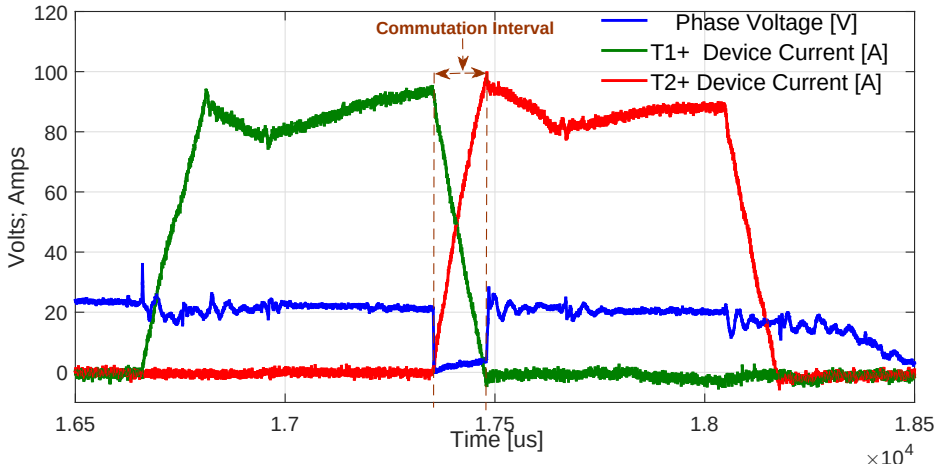

Fig. 3.40 Measured Current Waveforms During Natural Current Commutation

2. **Forced Commutation**: Here the out-going commutator device has to be gated off to force current to transfer to another part of the circuit. the current commutation is directly between active states and no intermediate commutation states are required as highlighted earlier in figure 3.8. This implies the use of power electronic devices with gate turn off capabilities such as Gate Turn Off Thyristors (GTOs), Integrated Gate Commutated Thyristors (IGCTs) or reverse blocking IGBTs or MOSFETS, for example. Figure 3.41 shows forced current commutation between adjacent machine commutator phases.

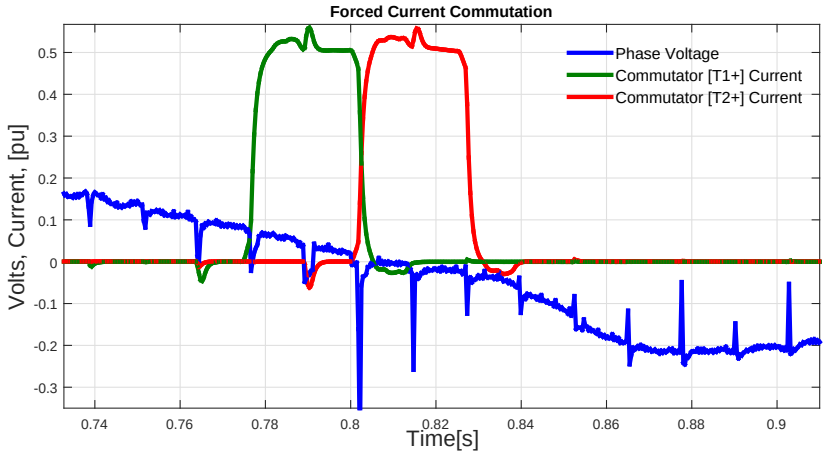

Fig. 3.41 Measured Current Waveforms During Forced Current Commutation

3. **Hybrid**: In this case a mixture of natural and forced commutation modes are applied whereby the current starts to naturally commutate from the out-going device to the in-going device by allowing an overlap (μ) when both devices are gated on. The current is then force commutated when it reaches a desired threshold mainly dictated by the amount of overlap inserted. Similar to the forced commutation mode, this mode requires devices with gate turn off capabilities. This mode can be exploited in applications where the switching devices' safe operating area imposes a maximum force commutated current limit e.g. if devices such as GTOs or IGCTs with unit gain turn off current limitations are used. In this case the current is allowed to naturally commutate to a level below the forced commutation current capability of the devices before the final forced commutation is applied. Figure 3.42 shows measured electronic com-

mutator current during hybrid current commutation between adjacent machine commutator phases.

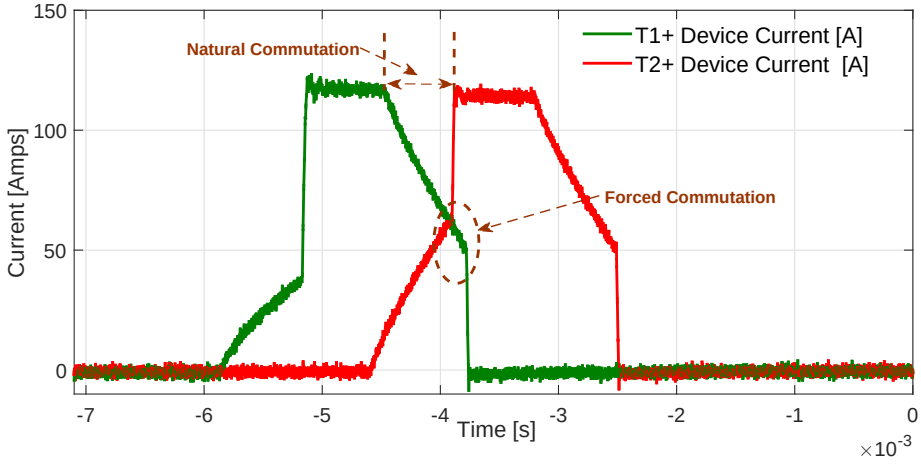

Fig. 3.42 Measured Current Waveforms During Hybrid Current Commutation

In comparison to brush commutated machines, these electronic commutation modes offer an extra degree of freedom which can be exploited to optimize the machine performance. For example, in applications where limitations are imposed on maximum forced commutation current the power electronic devices can safely handle, a mixture of natural and forced commutation i.e. hybrid commutation can be employed. In this case, the current is first naturally commutated to a value below the forced commutation capability of the devices before forced commutation is applied. This can ease the electronic commutator power device rating and gating requirements significantly if unity gain turn-off semiconductor devices are employed.

3.6.1 Electronic Commutator Fault Tolerance

Two main electronic commutator failure modes are short circuit faults and open circuit faults. Line fuses can be employed for short circuit fault protection by turning the short circuit fault into an open circuit fault. Machine open circuit faults can occur for example due line fuse operation or to failure of the gating electronics resulting in commutator power electronics devices failing to turn on when requested to do so. Simulation results have shown that the two level topology can tolerate phase open circuit commutator faults and continue to operate with minimal impact on performance,

thanks to flexibility of electronic commutator which can accommodate adjustments to the firing control strategy to mitigate the effects of phase open circuit faults. Figure 3.43 shows an illustration of the stator phases showing electronic commutator device T_{2+} open circuit fault.

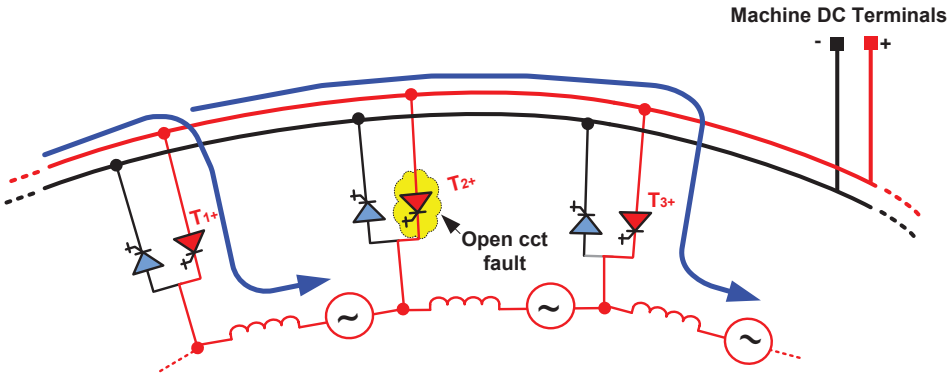

Fig. 3.43 Illustration of Machine Commutator Device Open Circuit Fault

Continuous machine operation can be readily achieved by inserting or increasing the commutator overlap angle of the commutator segments adjacent to the one with an open circuit fault (T_{1+} & T_{3+} in this case), to ensure there is always a commutator segment connecting the dc terminals to the machine at any given point. As such, the machine availability is greatly enhanced as there is no need of shutting down the machine in the event of such faults as the machine can continue to operate. This fault tolerance comes at the expense of increased dc link and machine torque ripple. The higher the number of stator phases the more tolerant the machine becomes to open circuit faults and the less the torque ripple. Figure 3.44 show simulated phase open circuit fault on a 24 phase machine, where phase 1 commutator device connecting the machine phase winding to the positive dc pole terminal is open circuited at *t=0.629s*. The figure highlights the impact of adjustments to the commutator overlap on the machine performance and ability to ride through the faults. The higher the overlap angle the better the ride through as can be seen in this figure. For a machine with N stator phases, the optimum overlap should be $\mu = 360/N$ degrees to ensure continuous path for dc current to bypass the open circuited phase *Iph 1* , in this case for N=24 implies overlap $\mu = 15$ degrees. Figure 3.45 shows the effect of overlap adjustment on

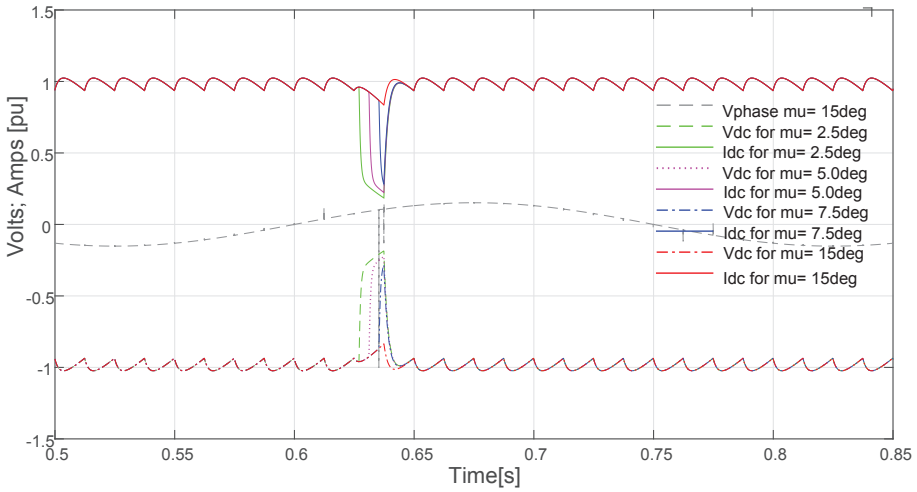

Fig. 3.44 Phase Open Circuit Fault: DC voltage & Current Waveforms for Different Overlap Angles Compensation

both the commutator phase current and machine phase winding current when riding through the fault. Its clear from this figure that when phase 1 fails to open circuit, the preceding phase *Iph 24* is extended to compensate for the failure.

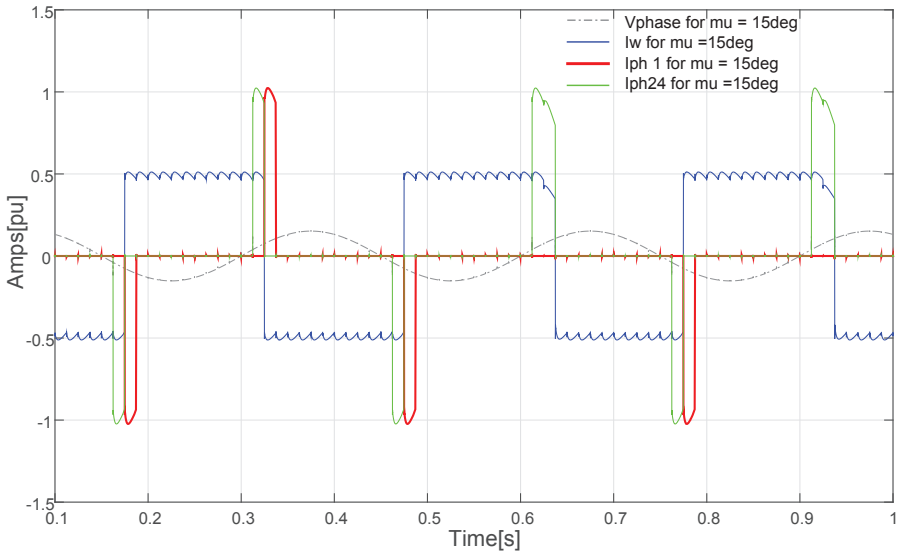

Fig. 3.45 Phase Open Circuit Fault: Current Waveforms Iw, Iphase 24, Iphase 1 & Phase Voltage for 15 Degrees Overlap Angle Compensation

3.7 Even and Odd Number Topology Comparisons

In order to fully characterise the advantages and disadvantages of even and odd numbered machine topologies, two designs were compared, one with an odd number of phases and the other with an even number of phases. For the even number topology, 24 stator phases was considered a good compromise between power electronics device utilisation and machine dc link ripple and torque ripple signature. For the odd number topology, the number of stator phases was chosen based on; (a) the machine has to have fewer number of phases compared to the even number topology, (b) the number of phases has to be a multiple of 3 to minimise the number of voltage sensors required to obtain a balanced three phase voltage set for the proposed machine and commutator control strategy, (c) the machine has to have similar or better dc link voltage ripple & torque ripple signature to that of the chosen even numbered machine. Based on these constrains, a 15 phase machine topology was chosen.

To enable a fair comparison, the two designs both had the same power rating 2MW, same machine stator diameter dimensions albeit with different number of slots, same number of rotor poles and the same number of turns per coil. The 24 phase machine was designed with 72 slots and full pitch coils. The 15 phase machine was designed with 90 slots and 1 slot short pitched windings. Simplified Matlab Simulink models of the 15 phase and 24 phase designs were developed and the comparative study results from these models are summarized in the next section. The following simplifying assumptions were made in the models:

1. *Commutator Devices*: The electronic commutators were modelled with forced commutation Gate Turn Off (GTO) devices with RC snubbers. The same safety factors were applied to the power electronic components used in this comparative study.

2. *Machine Flux*: The airgap flux distribution was derived from the 2D Finite Element (FE) models of the two machine designs.

3. *Back EMF*: The stator back Electromotive Force (EMF) induced in the coils was computed in Matlab from the machine design parameters.

4. *Armature Reaction*: Machine armature reaction effects were represented as simple triangular armature MagnetoMotive Force (MMF) waveforms.

5. *Constant Current Source*: The machines were fed from a constant dc current source mimicking the function of a current source rectifier supply.

6. *Machine Torque*: The machines airgap torque were computed from the back phase EMFs, the phase currents and machine operating speed.

7. *Electronic Commutator Losses*: The electronic commutator losses were computed using PLECS software thermal modelling tool and semiconductor device data sheet values.

3.7.1 Electronic Commutator Switching Devices Utilisation

A significant cost of the electronic commutator is in the power electronics switching devices. As such the switching device utilisation for the two topologies is an important factor. The switch utilisation ratio can be defined as;

$$U_{swt} = \frac{V_{max} I_{dc,max}}{q V_{gto} I_{gto}} \tag{3.20}$$

where; q is total number of commutator switching devices, V_{gto} and I_{gto} are the peak voltage and current ratings of the switching devices and $V_{max} I_{dc,max}$ gives the rated machine output power. Whole wafer Thyristor type devices such as GTO are considered the best candidates for this work owing to their high current rating capability for the low switching frequency duty required in this topology. For a given machine VA rating, reducing the number of devices should increase the either the phase current or voltage rating per device. As such the device utilisation should stay the same for a given machine VA rating. However, this work aims to employ commercially off the shelf power electronic devices and these come in discrete voltage and current ratings. For example commercially off the shelf asymmetric GTOs from semiconductor manufacturers e.g. ABB, Dynex come in two voltage ratings 2500V and 4500V and current ratings of 600A, 1500A, 2000A, 3000A, & 4000A. The power, voltage and current ratings of the two machines are given in table C.2.

Table 3.1 24 Phase and 15 Phase Machine Ratings

	24 Phase Machine	**15 Phase Machine**
Power (MW)	1.900	1.900
DC Voltage (V)	794 V	990 V
DC Current (A)	2400 A	1926 A
Phase Voltage (V)	100 V peak	200 V peak

As can be seen from table C.2 the voltage stresses are similar as the devices will commutate comparable dc link voltages. Analysis of the operational characteristics of these two topologies also show that for a given heatsink thermal impedance, similar thermal performance is obtained. Simulation of the semiconductor device losses, peak and average junction temperatures for rated conditions operation (see appendices) show that the same semiconductor devices can be used for both 15phase and 24 phase machines for the above rating without exceeding the devices safe operating area. Although the 24 phase topology results in high semiconductor device peak current due to high dc link current rating, its mean commutator phase current over a fundamental cycle is lower than that of the 15 phase topology. This is due to the fact that the 24

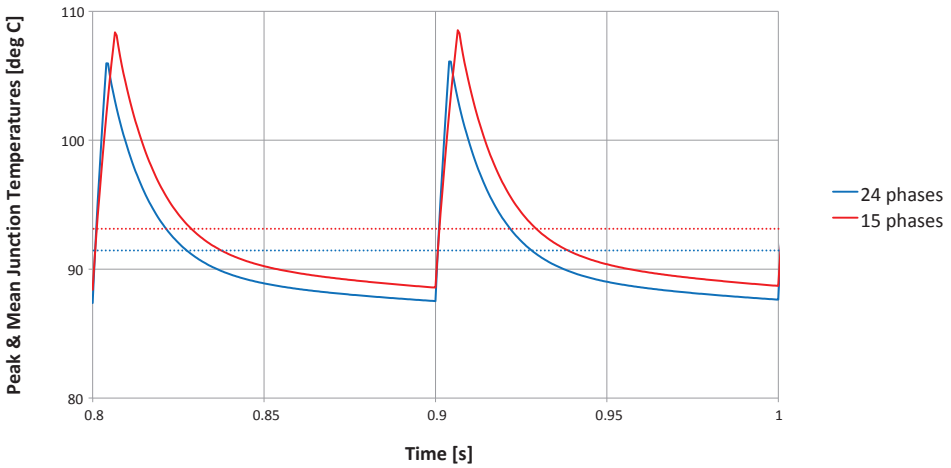

Fig. 3.46 15 Phase and 24 Phase Commutator GTO Peak and Mean Junction Temperatures at Rated Machine Speed and Rated Power

phase commutator devices conduct phase current for shorter durations compared to the 15 phase topology over a fundamental cycle. This results in lower peak junction temperature for the 24 phase compared to the 15 phase despite the higher peak phase current for a given heat sink thermal resistance. Figure 3.46 shows the simulated device peak junction temperatures and mean device temperatures for rated conditions operation when the same ABB GTO device 5SGA 15F2502 is used for both designs.

The same device rating safety margins were applied to both the even and odd number topologies. The utilisation factors for the electronic commutator switching devices are 0.017 and 0.011 for the 15 phase and 24 phase topologies respectively. The odd number topology has circa 35% improvement in device utilisation compared to the even number topology. The odd number of stator phase design offers better power electronic switching device utilisation in comparison to the even number of phase design due to reduced device count, $q = 30$ for odd number compared to $q = 48$ for even number topology in this case.

3.7.2 Commutating Inductance

As alluded to earlier, from a power electronic converter design & footprint reduction viewpoint, a lower commutating inductance is desirable. For odd numbered machines, only short pitched windings are permitted to eliminate circulating currents within the machine stator polygonal winding as shown in figure 3.16. In this case a coil side undergoing commutation shares a slot with another coil from a different phase that is not undergoing commutation. However, with a steady dc current in the coil not undergoing commutation there is effectively no coupling from that coil. As such all things being equal, short pitching should result in reduced commutating inductance as reported in [90]. However, for comparison with even numbered machine designs where the same number of turns per coil is maintained, an odd number design leads to considerably higher commutating inductance inspite of the short pitching. In this design the odd number topology had circa 4 times the commutating inductance compared to the even number topology. This is due to the fact that with the odd number of stator phases two short pitched coils are connected in series for each phase winding leading to a higher effective number of coil turns per phase and more phase end

winding overhang. As a result odd numbered designs tend to have higher commutating inductance compared to their even numbered counterparts.

3.7.3 Machine Torque Pulsations & DC Link Voltage Ripple

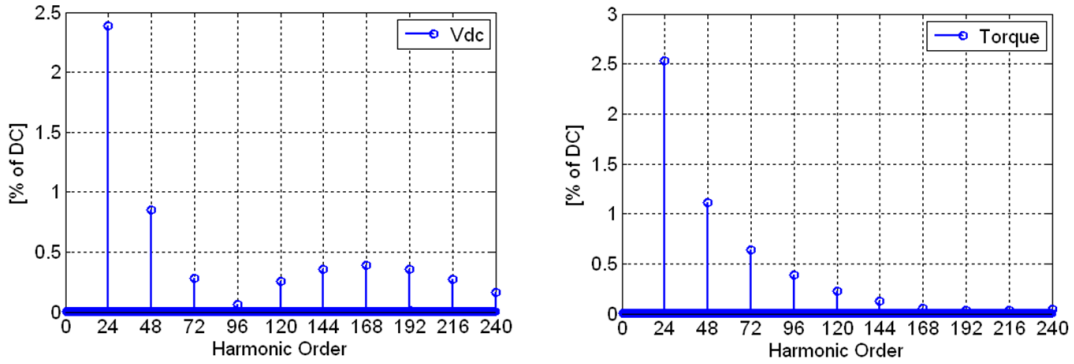

Fig. 3.47 Simulated 24 Phase Machine DC Link Voltage and Machine Torque Ripple Harmonic Orders

Its been highlighted earlier that one of the attractive features of this machine topology is that the electronic commutator devices switch at machine fundamental frequencies. As such, for a machine with N even number of stator phases, there are N simultaneous commutation events over a fundamental frequency cycle. This implies that the dc link voltage generated from the machine back electro motive force (emf) has the lowest dominant ripple harmonic at $N.f_s$, where f_s is the machine stator fundamental frequency. For example a 24 phase machine will have a significant dc link voltage ripple frequency of $24.f_s$ as highlighted in figure 3.47. The dc link voltage ripple has a direct impact on the size of any dc link inductor that is essential for any current source drive. Higher dc link voltage ripple will require a higher inductance value which can adversely affect the overall drive footprint and cost. Neglecting torque pulsations due to space harmonics of the machine winding function, it is also apparent that the dominant machine time harmonic will be at $N.f_s$ frequency as a result of N simultaneous machine current commutation events over a fundamental frequency cycle as highlighted in figure 3.47.

On the other hand, an attractive feature in the odd phase numbered machine is that the phase shift between the commutations of the devices connecting the machine phases to the positive and negative dc rails leads to $(2N)$ current commutation events

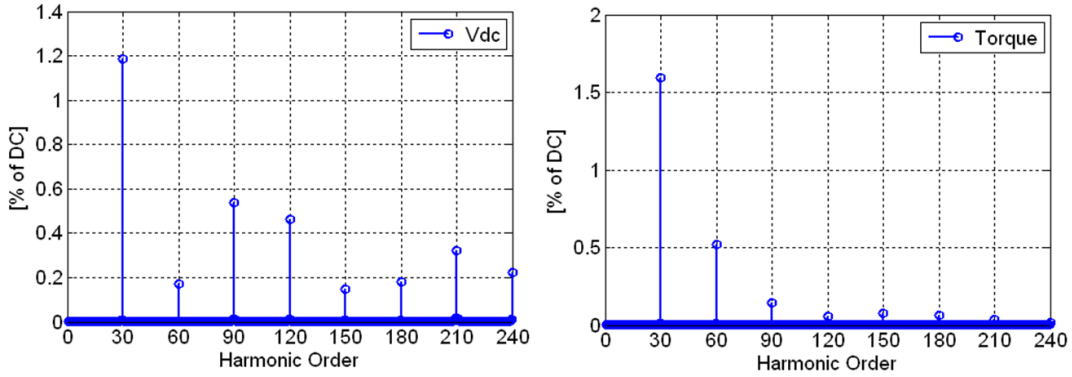

Fig. 3.48 Simulated 15 Phase Machine DC Link Voltage and Machine Torque Ripple Harmonic Orders

over a fundamental frequency cycle due to the interleaved commutator switching nature. This implies that the dc link voltage generated from the machine back electro motive force (emf) has a lowest dominant ripple harmonic at $(2Nf_s)$, where f_s is the machine stator fundamental frequency. For example, a 15 phase machine will have a significant dc link voltage ripple frequency of $30f_s$ as highlighted in figure 3.48. In comparison to the 24 phase even numbered machine, the odd numbered 15 phase machine yields an even higher dc link voltage ripple frequency despite the number of phases being almost half. This characteristic is highly desirable as it reduces the size of any dc link inductance that is essential with this current source drive type, yielding reduced overall drive footprint and cost.

Similarly neglecting space harmonics due to machine winding function, it is also apparent that the dominant machine time harmonic will be at $(2Nf_s)$ frequency as a result of $(2N)$ commutation events over a fundamental frequency as highlighted in figure 3.48. This means the dominant torque pulsation harmonic frequency is shifted to much higher frequencies where its impact is significantly reduced since its amplitude falls inversely with the harmonic order. Therefore, despite the odd number 15 phase machine having fewer phases, fewer power electronic commutator device count, it gives superior dc link voltage ripple and torque pulse ripple than a much higher even phase number 24 phase machine.

Figure 3.49 and figure 3.50 show simulated generator operation waveforms of 15 phase and 24 phase topologies. The figures show current waveforms of two adjacent

electronic commutator segments, machine phase winding currents & phase voltages and overall output dc link voltages.

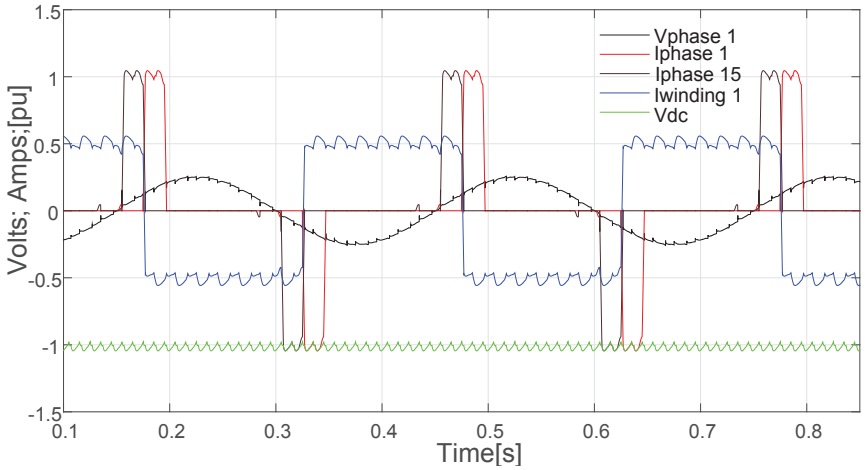

Fig. 3.49 Generating Mode: 15 Phase Topology Voltage and Current Waveforms

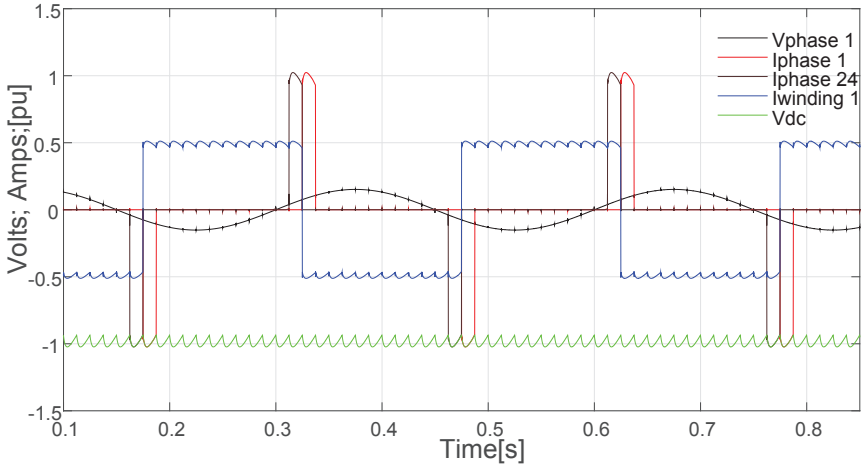

Fig. 3.50 Generating Mode: 24 Phase Topology Voltage and Current Waveforms

3.7.4 Electronic Commutator Losses

Mathcad and PLECS simulation software thermal toolbox was used to compute the electronic commutator devices switching, conduction and reverse recovery losses for the two designs at the same operating power levels. Detailed loss calculations for the comparisons presented here is given in the appendices. In this comparative study, the ABB asymmetric GTO device 5SGA 15F2502 (see appendices for data sheet) was used and the same heatsink was assumed in both designs. Figure 3.51 give a comparative summary of the electronic commutator losses for the two designs. The

individual commutator phase GTO conduction losses per device were found to be higher in the 15 phase machine. However, the total GTO conduction losses for the whole machine electronic commutator per fundamental cycle are lower than that of the 24 phase machine as shown in figure 3.51, thanks to the significant reduction in the number of semiconductor devices and better device utilisation factor of odd number topology. The auxiliary clamp circuit diode losses are significantly lower due to the reduced device count and also due to reduced commutation current $\frac{di}{dt}$ resulting from the higher commutating inductance. The turn off losses are also lower in the 15 phase topology due to the fact that the 24 phase machine design resulted in higher rated dc link current for the given machine constraints of size and number of turns per coil. Due to these reasons, the odd number topology has been shown to give a much better efficiency compared to the even number topology.

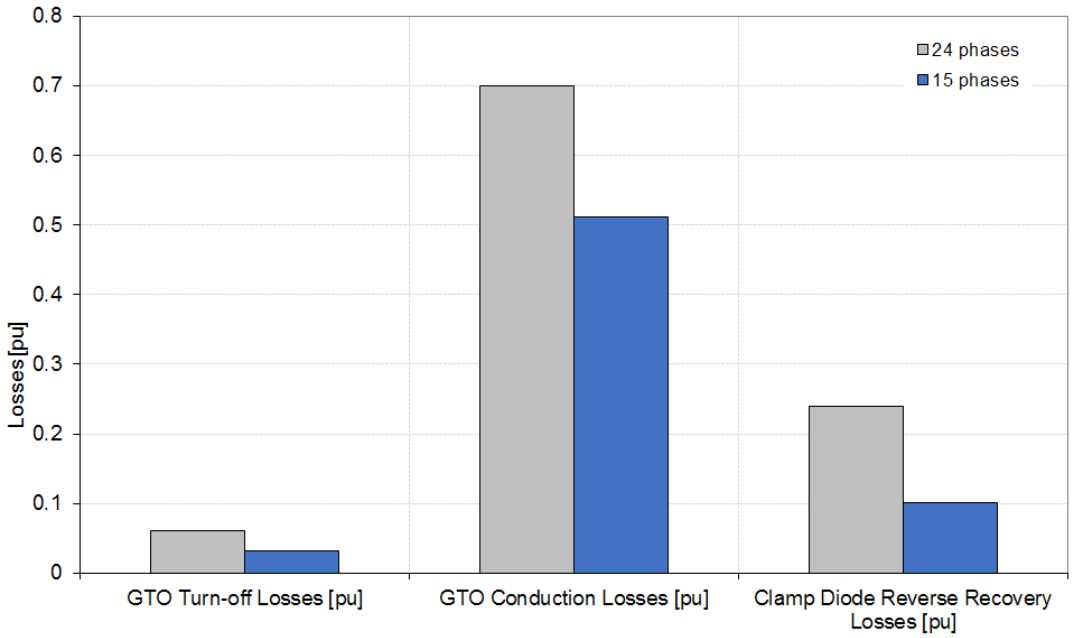

Fig. 3.51 Comparison of Electronic Commutator Power Electronics Device Losses

3.7.5 Electronic Commutator Footprint

For the electronic commutator footprint comparison, the electronic commutators were designed to give the same power rating, same safety margins and assumed the same liquid cooling method. Figure 3.52 shows the electronic commutator power electronics components footprint comparison by volume for the 2MW power rating for the two

topologies. The study has shown that the 15 phase electronic commutator gives an 8% volume reduction compared to a 24 phase equivalent. Although the number of devices is significantly less in the 15 phase topology, the overall volume occupied by the semiconductor switching devices has little impact on the total volume. However, the gating electronics and semiconductor cooling heatsink account for a very large part of the volume and their number is directly proportional to the number of phases. The study highlighted that the auxiliary commutation circuit clamp capacitors account for a significant volume of the electronic commutator with the highest volume on the 15 phase topology mainly due to the higher commutating inductance compared to the 24 phase topology. However, the overall footprint for the 15 phase topology is 8% less in volume compared to the 24 phase topology.

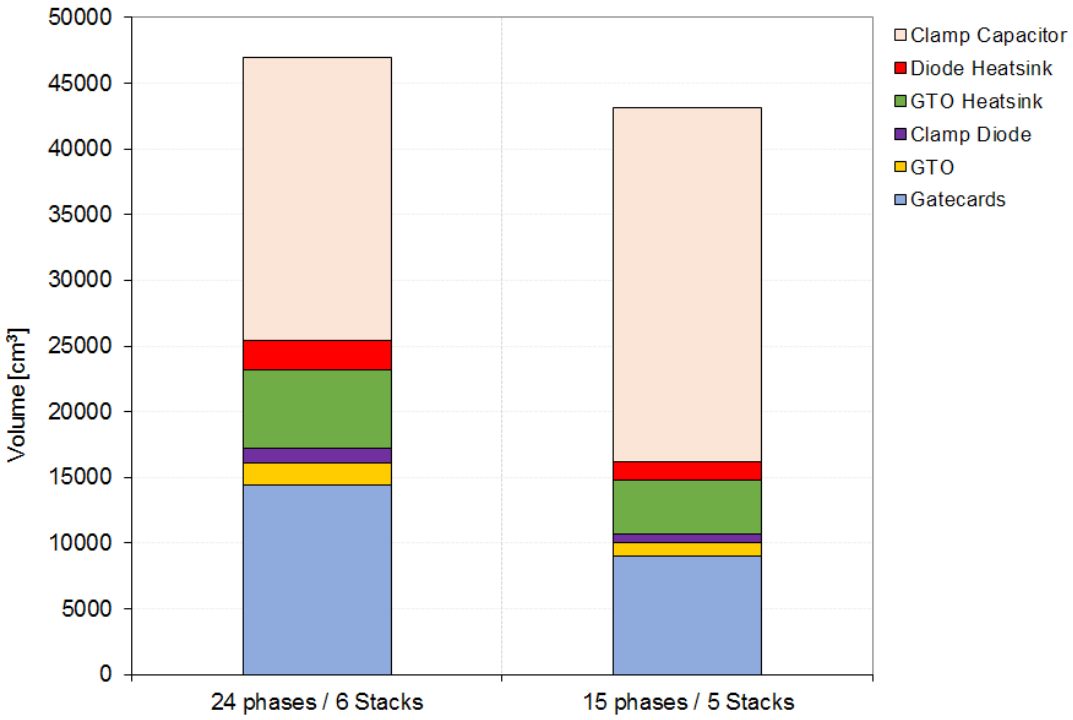

Fig. 3.52 Comparison of Electronic Commutator Power Electronics Volumetric Footprint

3.7.6 Electronic Commutator Protection

Fast fault detection is desirable to enable rapid shutdown of the electronic commutator in the event of a fault. Analysis and simulation study has shown that the clamp

capacitor voltage parity detection can effectively detect all faults within the electronic commutator and machine. Simulation studies have confirmed that, for even number topologies, the two auxiliary clamp capacitor voltages have the same amplitude and phase owing to the simultaneous commutation events on the two machine phases undergoing commutation at any given time. This implies that the clamp capacitors **C+** and **C-** will get charged and discharged at the same time. Thus;

$$|V_{c+}(t)| = |V_{c-}(t)| \tag{3.21}$$

where the clamp voltage can be expressed as

$$V_{c\pm}(t) = \pm(V_c(t_n) + \int_{t_n}^{t_{n+1}} (\frac{i_c(t)}{C_c})dt) \tag{3.22}$$

where $V_c(t_n)$ is the clamp capacitor voltage just before clamp diode current commutation starts, $i_c(t)$ is the clamp capacitor current and t_n & t_{n+1} are time instances between successive phase commutation events.

It can be easily inferred from (3.22) that if simultaneous current commutations do not occur on the positive and negative clamp rails (indicative of malfunction of the commutator), the currents through the positive and negative clamp capacitors $i_c(t)$ will not be the same and consequently (3.21) will not hold true. This feature can be employed for fast detection of electronic commutator open circuit and short circuit faults by comparing the amplitudes and phases of the two clamp circuit rail voltages against predefined thresholds.

Figure 3.53 shows equal clamp capacitor voltage waveforms and the resultant divergence at *t=1.18s* when a phase electronic commutator device fails to turn on (open circuit fault).

However, with an odd number of stator phases, the clamp capacitors **C+** and **C-** can not be charged and discharged at the same time owing to the interleaved control strategy discussed earlier. In fact the positive and negative clamp capacitor rail voltage waveforms are the same in amplitude but phase displaced by (π) radians as shown in figure 3.54. As a consequence, the protection scheme described for the even phase number topology when applied to machines with an odd number of stator

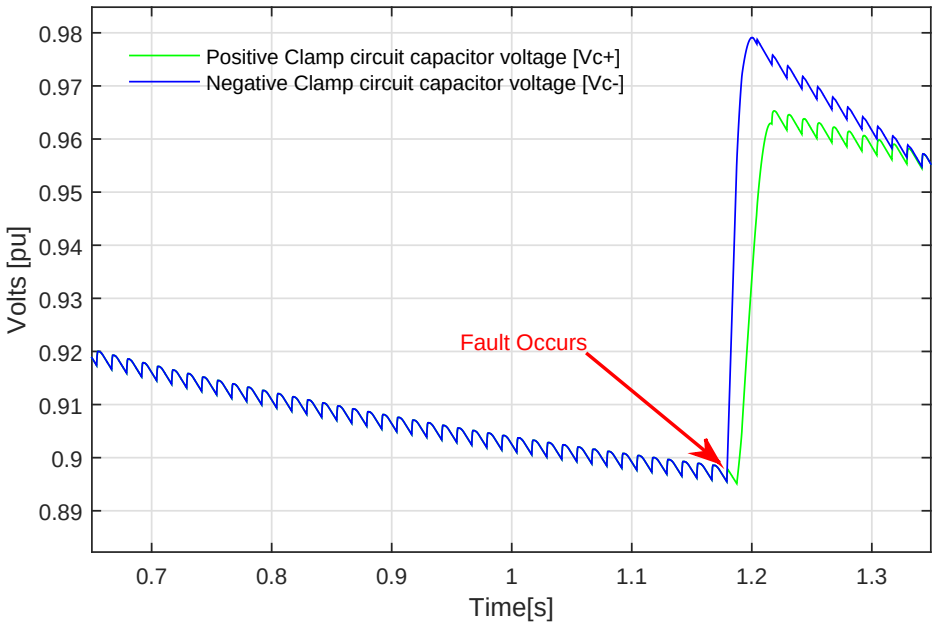

Fig. 3.53 Even Number Topology: Simulated Clamp Capacitor Voltage Divergence When Commutator Fault Occurs

phases must be modified to account for the inherent phase shift between the clamp voltages as shown in figure which highlights simulated phase open circuit failure. Consequently the response of this protection scheme is somewhat slower and less effective in comparison to even numbered stator phases.

3.7.7 Odd Stator Phase Number Topology Advantages

In comparison to the 24 phase design, the 15 phase design was found to have the following advantages:

1. *Semiconductor Device Losses*: 30% less devices in terms of power semiconductors, electrical passive components, gate cards and cooling heat sinks. The same power semiconductors can be used for both machines, hence the 15-phase electronic commutator is considerably cheaper and more reliable.

2. *Semiconductor Device Utilisation*: Better switching device utilisation resulting in more compact electronic converter design due to reduced power electronic devices count, so easier to integrate the power electronics to the machine.

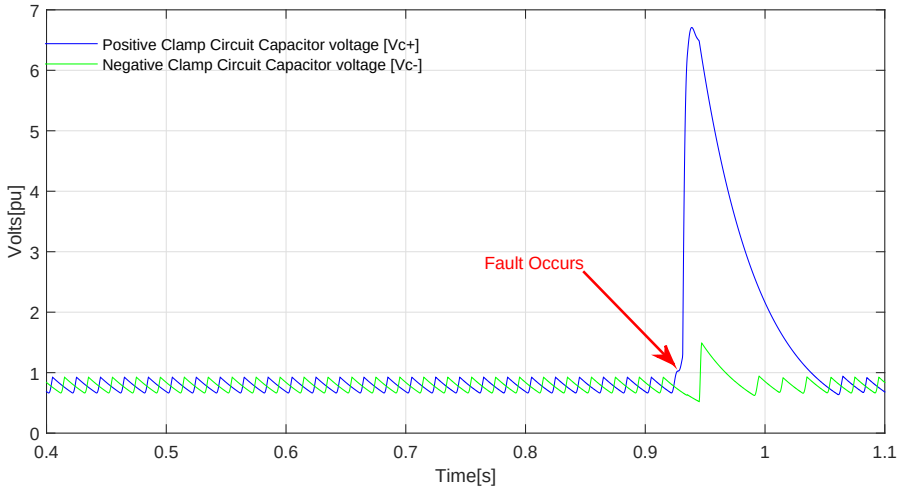

Fig. 3.54 Odd Number Topology: Simulated Clamp Capacitor Voltage Divergence When Fault Occurs

3. *Rated Current*: Higher DC link voltage due to two seriesed short pitched windings per phase, resulting in a lower DC link current for the same power rating. This however comes at the expense of increased operating dc link voltage for a given power rating.

4. *DC Voltage Harmonics*: Significantly less DC link voltage ripple due to the interleaving commutator operation which resulted in a higher ripple frequency with lower harmonic amplitudes.

5. *Machine Torque Ripple*: Significantly less air gap torque ripple due to the interleaving commutator operation.

6. *Overall Electronic Commutator Losses*: Less total electronic commutator power dissipation i.e. sum of power semiconductors conduction & switching losses and clamp diodes reverse recovery losses.

3.7.8 Odd Stator Phase Number Topology Disadvantages

In comparison to the 24 phase design, the 15 phase design was found to have the following disadvantages:

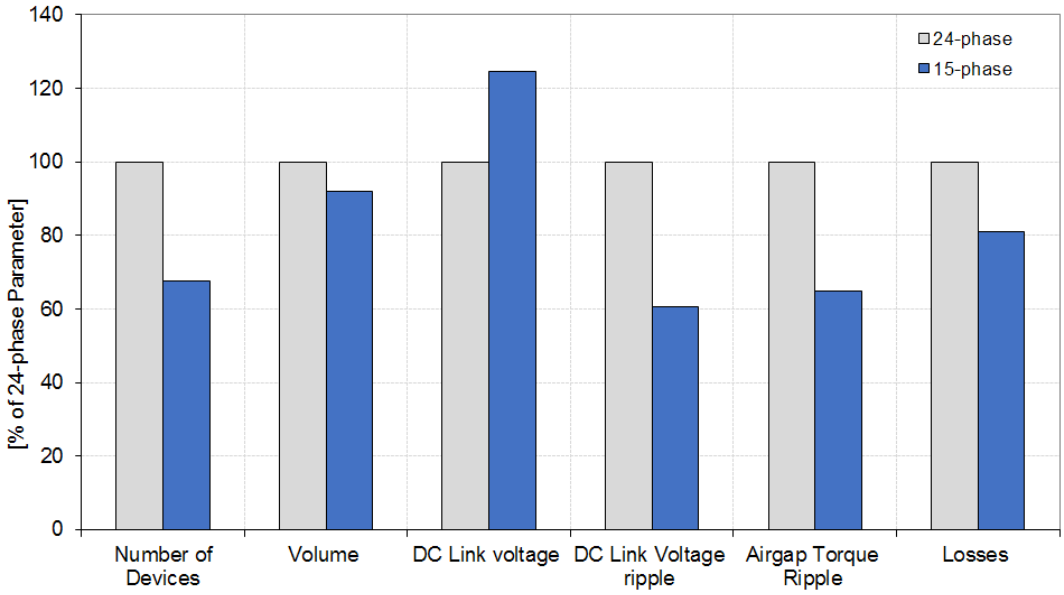

Fig. 3.55 Figure of Merit Summary: Comparison of 24 Phase and 15 Phase Designs

1. *Commutating Inductance*: Higher commutating inductance due to the high number of turns per phase winding, bearing in mind that inductance is directly proportional to the square of the number of turns.

2. *Auxiliary Clamp Capacitance*: Higher clamp capacitance required to achieve same clamp voltage due to the increased commutating inductance requiring more commutation energy absorption, so the clamp capacitors are bigger.

3. *Power Dissipation*: Owing to higher commutating inductance, more power ($\frac{L_c I^2}{2}$) dissipated into the clamp discharge circuit. However, the clamp discharge resistor power dissipation represents only 10% of the total electronic commutator losses in the case of the 24-phase machine. This drawback can be mitigated by use of energy recovery circuits.

4. *Fault Detection*: Clamp Voltage Imbalance protection scheme proposed to detect electronic commutator failure or malfunction has reduced response bandwidth due to the asymmetric nature of the commutator operation with an odd phase numbered machine.

Figure 3.55 gives a figure of merit summary of the comparisons between even and odd number of stator phases for a 24 and a 15 phase machine. The comparison

is normalised on the 24 phase design parameters. Although the analysis and comparison was done on two specific design, the parameters used in the figure of merit assessment follow a similar trend for generic even and odd number topologies of similar performance. In general, the benefits of odd-phase number topology in terms of cost, reliability and air gap torque ripple outweigh its drawbacks and is an attractive alternative proposition to the even numbered topology.

3.8 Summary

This chapter has presented the operating principles and analysis of the electronic commutation process of the multiphase electronically commutated dc machine topology with an even number of stator phases. The simulation and analysis was extended to a topology odd number of stator phases. The current commutation processes for both topologies were analysed and key factors affecting electronic current commutation presented. It was shown that symmetric current commutation control proposed for the even stator phase number electronic commutator topology can not be used for the odd phase number topology. Instead, the study has shown that an interleaved current commutation control strategy proposed aided suppression of net circulating current in the stator polygonal winding for the odd number topology. Interestingly, the fast Fourier transform of the phase winding current of a 15 phase machine revealed the absence of the 15^{th} harmonic current component, which would otherwise have resulted in a net circulating current in the stator polygon. Fast Fourier transforms of the simulated dc link voltage and machine torque has confirmed that despite the use of squarewave phase current excitation, low order harmonics had no detrimental effect on the machine torque ripple signature. In fact, the lowest torque ripple harmonic order components where shown to be Nf_s and $2Nf_s$ for even and odd number respectively, where N is the stator phase number and f_s is the machine fundamental frequency.

A comparative analysis based on two similarly rated even and odd number topologies was given and figure of merit summary highlighted that similar or even better performance to the even stator phase number topology can be obtained using odd stator phase number topology with significantly less number of stator phases.

Its envisaged that the two level topologies introduced in this chapter will be applicable to low and medium voltage applications where commercially off the shelf power electronic switching devices can be directly applied without the need for series connection of switching devices. However, a limitation of these two level topologies is that in applications that require high dc link voltages, series connected power electric devices will be required, as such dynamic and steady state voltage sharing of seriesed devices will be required. The next chapter will analyse a variant of the multiphase electronically commutated dc machine topology that is better suited to high voltage applications and circumvents the need for direct series connection of electronic commutator devices.

Chapter 4

Multi-Level Multiphase Electronically Commutated DC Machine Topology

4.1 Introduction

The two level multiphase electronically commutated dc machine presented in the preceding chapters is well suited for low voltage applications. For high voltage applications, the two level topologies require series connection of commutator devices which brings some challenges in ensuring transient, dynamic and steady state voltage sharing across the string of series connected devices. An alternative topology suitable for high voltage dc application which benefits from most of the advantages of multiphase electronic commutated dc machines alluded to earlier is the multilevel multiphase electronically commutated dc machine topology. This topology was invented by Allan Crane as reported in [92]. The work presented in this chapter is a scientific analysis of the operational attributes of this topology. This work seeks to analyse and evaluate suitable electronic commutator configurations and their associated control schemes for this multilevel topology. In this analysis, suitable control schemes and simulation models are developed and energy recovery circuit topologies are proposed for recovering commutation energy back into the drive circuit. Control strategies aimed at enhancing the fault tolerant operation of this topology are proposed and simulation results presented.

4.2 Brief Review of Multilevel Converters

In todayś dc systems, Pulse Width Modulated (PWM) Voltage Source Converters (VSC) based on Insulated Gate Bipolar Transistor (IGBT) device technology are widely used in ac/dc conversion stages. These PWM controlled VSC offer several benefits such as; low torque pulsations and superior harmonic performance in comparison to LCIs [93] but suffer the fault current limitation drawback owing to the inherent of free-wheeling diodes when applied to dc systems. However, an attractive feature of recent VSC topology for medium to high voltage applications is the so called multilevel converter topology.

The multilevel concept enable converters to be built using Commercially Off the Shelf (**COTS**) low & medium voltage power electronic devices to achieve high output voltages that would otherwise require series connection of string of devices, which bring with it problems of static and dynamic voltage sharing amongst the seriesed devices [94–96]. However, an undesirable feature of most multilevel VSI is that of capacitor voltage balancing and energy balance within the multilevel cells [53], [97], [98]. Several investigations have been reported to address these issues but most of these require extra capacitor voltage balancing hardware circuits or incur some control modulation margin reserve penalty for capacitor voltage balancing algorithms [99]. Other researchers [100],[101] have proposed alternative modular multi-level generator topologies to address neutral point stability and capacitor voltage balancing issues of multilevel VSI topologies. However, their work is based on the premise of direct connection of the generator to the ac grid and involves ac/dc, dc/dc and dc/ac conversion stages for each generator circuit. For power delivery system applications where the generators can deliver high dc voltages directly or do not require direct connection of generator output to the ac grid such as dc systems, these additional conversion stages are not necessary.

In some cases, multilevel topologies can lead to reduced reliability due to high component count in comparison to standard two level converter topologies. However, the introduction of fault tolerance through multilevel concepts can enable the overall availability of the system to exceed that of the two level topologies as the system can still be operated with one or more faulty cells as reported in [102, 103]. Although

failure of any one phase-switching module unit does degrade system performance somewhat, the urgency for immediate repairs is reduced since system shutdown is not required. This is attractive for power delivery systems deployed in remote or harsh and not readily accessible sites, such as wet renewable or offshore renewable power systems. For such systems, the concept of multilevel converters is still attractive and more research is required to come up with suitable and reliable power electronic topologies that can address the short comings of existing multilevel VSIs for dc power systems. A detailed review of multiphase machine/converter topologies applicable to wind energy conversion systems has been presented in [28]. However, all these topologies are limited to the conventional ac machine topologies. The topologies analysed here represent a shift from these conventional ac machine topologies.

4.3 Multilevel Multiphase Machine & Converter Topology Description

Having alluded to the potential benefits of multilevel machine and power electronics topologies of current source type for dc systems in section 1, this section briefly outlines the multilevel machine/converter topology operating principle and highlights its desirable attributes when applied to dc systems. The multilevel topology feature stator windings comprising of a plurality of coils in the winding slots forming a plurality of stator phases significantly greater than three. Unlike the 2-level topologies discussed so far where the connections between adjacent machine stator phases form a continuous polygonal ac machine stator winding, here each stator phase winding is terminated in a power electronic switching module and connects to the adjacent stator phase winding in dc domain through the dc output terminals of the power electronic switching module as highlighted in figure 4.1. Thyristor type devices are shown in this figure for illustrative purposes only, any power electronic devices with reverse voltage blocking capabilities are equally applicable. The auxiliary switching circuits shown in the figure may be necessary depending on the choice of power electronic semiconductor switching devices used, for snubbering action or for commutation energy recovery.

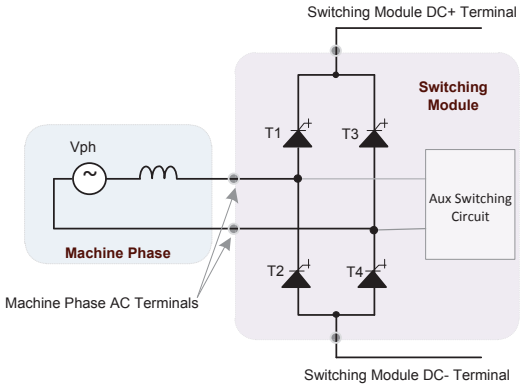

Fig. 4.1 Machine Phase & Switching Phase Module of the Multiphase Multilevel Topology

The dc terminals of each switching module connects to an adjacent phase switching module dc terminals as shown in figure 4.3. The series & parallel connected switching modules form a multilevel converter/machine structure where each machine phase winding sequentially connects to the module output positive (+ V_{dc}) and negative (-V_{dc}) poles through its switching power electronic module. Each switching module's dc voltage is only a small fraction of the total machine's output dc link voltage and is inversely proportional to the number of stator phases or switching modules connected in series, hence the multi-level topology.

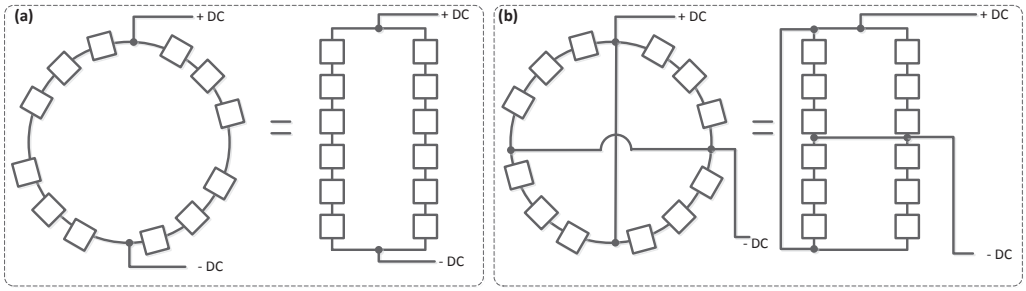

Fig. 4.2 Multiphase Multilevel Machine showing: (a) Two Commutator Parallel Paths & Four Commutator Parallel Paths Configurations

The two end terminals of a plurality of seriesed switching module sections can be connected in parallel with one or more similar sections to form the overall machine dc output terminals as shown in figure 4.2. Figure 4.3 shows two parallel paths arrangement similar to (a) in figure 4.2. Analysis of the operating modes of this topology reveal that, the switching events for the machine phase modules that are 180

electrical degrees out of phase have to occur simultaneously with mirrored antiphase switching events. For example, phases V_{1+} and phase V_{1-} in figure 4.3 are displaced 180 degrees around the stator and their induced stator phase voltages are in antiphase. As such, the mirrored antiphase switching events for the corresponding switching modules must occur simultaneously for symmetrical balanced machine operation.

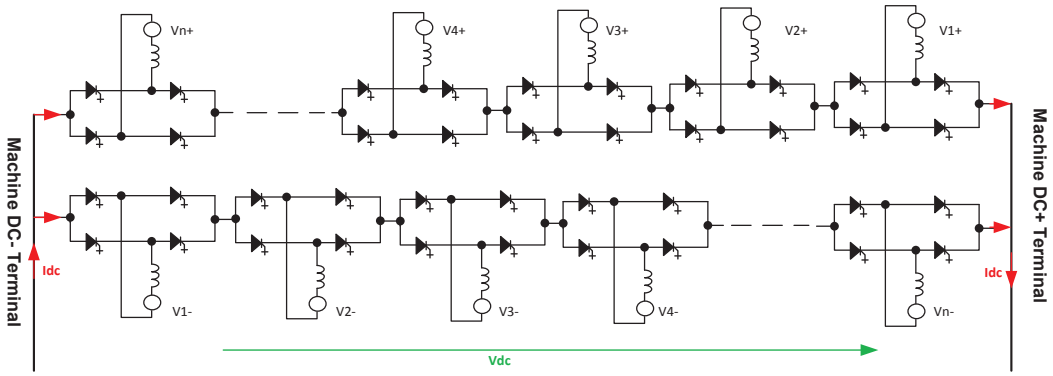

Fig. 4.3 Multi-Level Electronically Commutated DC Machine Topology

4.3.1 Multilevel Multiphase Topology Benefits

Analysis of the proposed multilevel multiphase topology has shown that the following benefits can be obtained in comparison to conventional topologies;

1. *Use of COTS Low Voltage Devices*: Owing to the multilevel structure, the topology facilitates use of lower voltage insulation system in the power electronics switching module construction, leading to reduction in the voltage isolation required for semiconductor devices.

2. *Machine Insulation Rating*: Since the phase switching modules are interconnected in the dc domain, the main machine phase winding to wall insulation is dominated by a dc voltage component with substantially less significant ac component. As such, the phase inter-turn coil insulation duty is reduced and the main wall insulation can employ simple self stress grading insulation systems, thus easing the insulation duty requirements and facilitating manufacturing.

3. *Switching Frequency & Device Losses*: This topology also benefits from the low switching frequencies since the phase switching module devices only switch at the machine fundamental frequencies which are inherently low as discussed in previous chapters. As a consequence, semiconductor switching devices optimised for low conduction losses can be employed to yield very high efficient drives since switching losses are less significant in comparison to equivalent PWM controlled topologies. No detailed loss comparison was done between multilevel topology and the two level topology presented earlier. Its envisaged that the use of low voltage rated wide-band gap semiconductor devices in this topology can potentially yield efficiency benefits.

4. *Machine Torque Ripple*: The multiphase machine approach offers improved machine torque harmonic performance owing to the increased number of stator phases which inherently eliminates low order harmonics and shifts the remaining undesirable harmonics to higher orders where their undesirable impact on machine performance diminish with increasing stator phase number as alluded to earlier.

5. *Modular Design*: A modular phase switching module design facilitates manufacturing, cost reduction, faster product development and easy maintenance. The modular approach will enable integration of the phase switching modules with the machine to yield compact designs and eliminate cabling requirements between converter and machine.

6. *Drive Availability*: The overall drive system availability can be greatly enhanced due to redundancy and fault tolerance capability that can be designed into multiphase and multilevel topology.

4.4 Passive Commutator Topology Analysis

In applications where lowest cost, simplicity and high reliability of the power switching modules is required, simple diodes can be used as the H-bridge semiconductor devices in this proposed topology. Such passive topologies have been explored for conventional machine topologies [104],[105]. A limitation of the passive topology is that lack of

control of the power electronic converter, as a consequence the topology is only suitable for generator applications.

4.4.1 Full Wave Passive Topology

In this topology, the H-bridge switching modules are connected as shown in figure 4.3 but with passive diodes employed instead, where each phase winding is terminated in an H-bridge and the H-bridges in turn are cascaded in series to form a multilevel converter system. At least two parallel current paths are needed for the complete machine configuration. Unlike the two level topologies discussed earlier where the ac phase power electronic switching devices carry the full dc current, in this case the dc link current splits two ways and each machine phase winding and its corresponding H-bridge power electronic module only caries half of the dc link current as illustrated by simulated waveforms in figure 4.5 where the H-bridges and machine phases only carry half the dc link current. Other connections with multiple parallel paths are possible, however this will be at the expense of reduced output dc link voltage for a given machine stator phase number. With uncontrolled single phase commutator topologies, half wave or full wave H-bridge topologies are possible. Half wave topology has been discounted here owing to its high ratio of ac source VA rating to DC power rating, i.e. very low operating power factor and also its undesirable ability of produce a dc component in the ac source current.

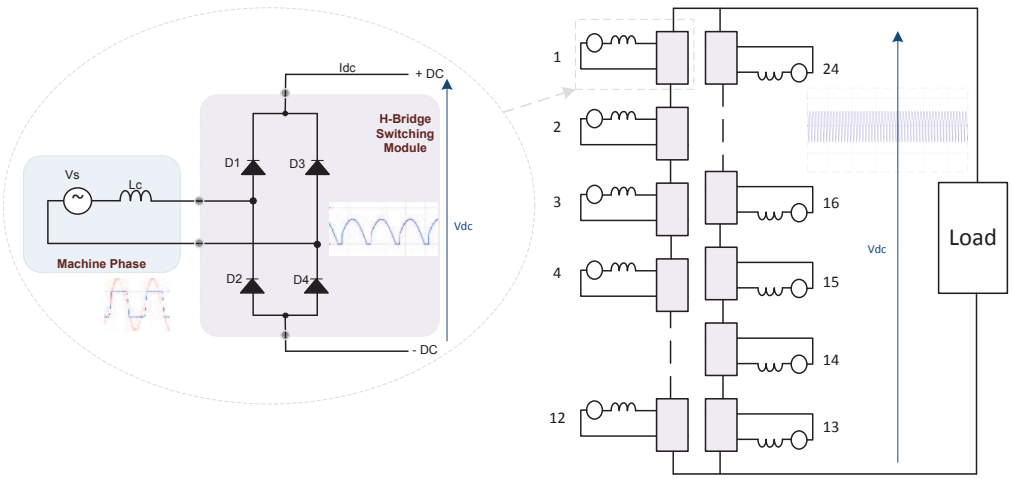

Fig. 4.4 Schematic Circuit of a 24 Phase Multiphase Generator & Phase H-bridge Cell.

4.4.2 Current Commutation

In this current source type topology, only natural current commutation occurs in the machine phase H-bridge switching phase modules. Its clear that when no commutation is taking place, the voltage drops across the machine inductance is zero due to the constant dc load current constraint. When the diodes commutate, the ac volts appear across the commutating inductance (L_c). An expression of the commutating interval can be readily obtained by integrating the equivalent inductor voltage equation over the commutation interval (μ) for the current commutating between positive and negative dc current ($+I_{dc}$ to $-I_{dc}$) & vice versa to give;

$$\mu = \arccos(1 - \frac{2\pi f L_c I_{dc}}{V_s}) \tag{4.1}$$

where V_s is the peak ac voltage, L_c is the phase commutating inductance, I_{dc} is the dc link current. The H-bridge average output dc voltage can be found by integrating the voltage over half time period and subtracting the volt-radian area lost every half fundamental cycle due to commutation to give;

$$V_{dc} = \frac{V_s}{\pi}(1 + \cos\mu) = \frac{2V_s}{\pi}(1 - \frac{2\pi f L_c I_{dc}}{V_s}) = V_{dc0}(1 - \frac{2\pi f L_c I_{dc}}{V_s}) \tag{4.2}$$

where V_{dc} is the average dc output voltage, V_{dc0} is the maximum possible rectifier output voltage, f is the ac fundamental frequency.

The per unit commutating reactance or reactance factor ($\frac{2\pi f L_c I_{dc}}{V_s}$) in (4.2), has a significant effect on the rectifier characteristics such as; output voltage regulation, harmonics in the ac input and dc waveform and power factor. From (4.2) above, the undesirable effect of commutating reactance is obvious on output voltage regulation. The per unit commutating reactance also changes the shape of the ac current waveform to the detriment of the power factor. It is important that the per unit commutating reactance is minimised in the machine design to alleviate its detrimental effects on the performance of the drive for this topology. There is a tradeoff however, the machine size tends to increase as commutating reactance decreases for a given type of motor design [106]. Therefore, to decrease the size and weight of a given machine, the machine design may lead to an increase in its reactance. However, in some cases a

higher commutating inductance aids fault current limitation which can facilitate use of power electronic devices with a lower current rating, otherwise fault current limiting measures such as line fuses may be required for protection.

A dc link choke is necessary between the generator dc output and the rest of the power delivery system load/network bridge converters to filter harmonics and reduce the dc link current ripple. As alluded to earlier, increasing the number of machine stator phases shifts the lowest dominant dc link harmonics to higher orders where their amplitude diminish with increasing phase number. This characteristic helps ease the requirements on the required dc link inductance to meet a given ripple current target.

The dc link choke inductance (L_{dc}) is typically sized to give the desired ripple current on the dc link [107] as;

$$L_{dc} = \frac{V_h}{2\pi f_h I_h} \tag{4.3}$$

where; V_h is the harmonic voltage amplitude at the dominant harmonic frequency f_h, which causes the dominant harmonic h of current I_h in the dc link. The target amplitude of the dominant harmonic current can be expressed as fraction of the rated dc link current (I_{dc}, such that $I_h = I_{dc} I_{h_{(p.u)}}$). In order to minimise the size of the dc filtering inductance, its important to minimize the amplitude of the harmonic voltage V_h as well as shifting its harmonic order to higher frequencies. Expressing the overall machine output dc link voltage as a Fourier series helps to highlight the impact of increasing stator phase number on both the order and amplitude of the harmonic voltage V_h and the overall output dc characteristic of the multiphase/multilevel topology.

4.4.3 DC link Harmonics

Single H-Bridge Output Voltage

To characterise the harmonic composition of the output dc voltage of this multilevel topology, the output of each single H-bridge can be expressed in terms of input by spectrum multiplication. For purposes of exploring the dominant dc link harmonics and simplifying the analysis, the machine phase commutating inductance will be neglected as its effects are considered secondary in comparison to those of the multiphase

multilevel circuit topology as far as dominant harmonics are concerned. For this current source converter topology, the output dc link current I_{dc} will be assumed constant. The output dc link voltage $V_{dc}(\theta)$ of a single H-bridge can be expressed as function of the input ac voltage $V_i(\theta)$ as;

$$V_{dc}(\theta) = S(\theta)V_i(\theta) \tag{4.4}$$

where $S(\theta)$ is a function associated with the conduction state of the H-bridge switching devices such that its amplitude has $\pm$ unit amplitude when its associated switching device is ON and zero all other times.

If the converter switching losses are neglected, using the power balance between converter input and output gives;

$$I_i(\theta)V_i(\theta) = I_{dc}V_{dc}(\theta) \tag{4.5}$$

Using the switching function $S(\theta)$ in (4.4) and substituting in (4.5), the input current $I_i(\theta)$ can be expressed as a function of the output current as;

$$I_i(\theta) = S(\theta)I_{dc} \tag{4.6}$$

If $S(\theta)$ is known then the dc link voltage $V_{dc}(\theta)$ can be determined. For a single phase H-bridge rectifier operating modes, $S(\theta)$ can be expressed as a Fourier series as;

$$S(\theta) = \frac{A_0}{2} + \sum_{i=1,2,3,\ldots}^{\infty} (A_n \cos(n\theta) + B_n \sin(\theta)) \tag{4.7}$$

Owing to the inherent half wave symmetry in an H-bridge, (4.7) simplifies to;

$$S(\theta) = \frac{4}{\pi} + \sum_{i=1,3,5,\ldots}^{\infty} \frac{\sin(n\theta)}{n} \tag{4.8}$$

For a machine with N stator phases, the machine phase n induced back emf can be expressed as;

$$V_n(\theta_i) = V_s \sin(\theta_i - \frac{2\pi}{N}(n-1)) \tag{4.9}$$

From the above, the dc link voltage for a single H-bridge $V_{dc_1}(\theta_i)$ for phase one can be obtained by multiplying (4.8) by (4.9). Simplifying the result using trigonometric manipulation yields;

$$V_{dc_1}(\theta_i) = \frac{4V_s}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin(\theta_i)\sin(n\theta_i)}{n} = \frac{2V_s}{\pi}(1 - 2\sum_{k=1,2,3,\ldots}^{\infty} \frac{\cos(2k\theta_i)}{4k^2-1}) \quad (4.10)$$

The 1st part of the final simplified expression is the average dc component, the second part is the ripple component which as can be seen from this term the dominant harmonic is a second harmonic of the phase fundamental frequency. Its also clear from (4.10) that only even harmonics are present in the output dc voltage.

Multilevel Machine DC Output Voltage

In this multiphase multilevel topology each single phase H-bridge can be assumed to preserve its own dc voltage and operate independently of other H-bridges. As such, the analysis of the overall machine output dc performance characteristics simplifies to a process of addition of the seriesed bridges in the correct phase relationships. Thus, the total output dc link voltage for a machine with N stator phases is the sum of the dc link voltages of all the H-bridges connected in series. For example, the dc link voltage of one string of bridges connected in series is given by;

$$V_{dc_{(N)}}(\theta_i) = V_{dc_1}(\theta_1) + V_{dc_2}(\theta_2) + V_{dc_3}(\theta_2) + \cdots + V_{dc_{(N/\gamma)}}(\theta_n) \quad (4.11)$$

where, $\theta_n = \theta_i - (n-1)\frac{2\pi}{N}$ and γ is the number of parallel circuits connected in series for $\gamma \geq 2$ for this multilevel topology. Note, when $\gamma = 2$ the output dc voltages on the two parallel strings will be identical both in amplitude and phase due to machine symmetry.

Substituting (4.10) for each phase dc output voltage expression in (4.11) and simplifying gives the Fourier series expression for the resultant dc link voltage for a machine with N stator phases as;

$$V_{dc_N}(\theta_i) = \frac{V_s N}{\pi}(1 - \frac{2\gamma}{N}) \sum_{k=1,2,3,\ldots}^{\infty} \frac{\cos(2k(\theta_i - (\frac{N}{2}-1)\frac{\pi}{N}))}{(4k^2-1)} \frac{\sin(k\pi)}{\sin(\frac{2k\pi}{N})} \quad (4.12)$$

where $\gamma \geq 2$.

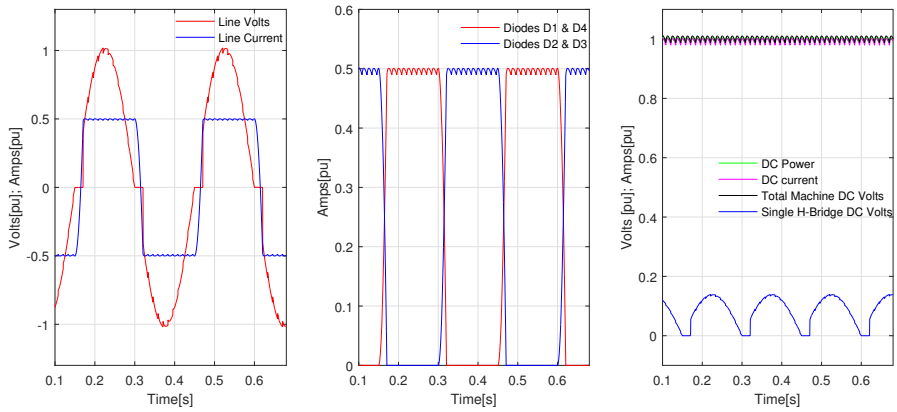

Fig. 4.5 Showing (a) AC Phase Voltage & Current, (b) H-bridge Diode Currents, (c) Output DC Voltage & Total 24 Phase Machine Output Voltage & Current.

The above expression highlights that the machine output dc voltage contains a steady dc component and an infinite but converging series of ac ripple harmonic components. Its obvious from the above expression that for a given stator phase terminal voltage, higher overall machine output dc link voltage can be achieved by increasing the number of stator phases. Since the phase voltages of each H-bridge are phase displaced by $(2\pi/N)$radians from the adjacent bridges, phase displacements exists between the output dc ripple voltages of the seriesed bridges. This inherent phase displacement results in cancellation of certain harmonics in the overall machine dc output voltage. Figure 4.6 shows the graphical representation of (4.12) for increasing phase number for a given ac phase voltage. For example, a single bridge has a dominant second harmonic whilst a machine with 24 phases with $\gamma = 2$ has a 24^{th} harmonic component as the lowest dominant harmonic on the machine output dc link voltage. Figure 4.5 shows simulated dc link output voltages for a single phase bridge and a 24 phase machine with two parallel connected paths $(\gamma = 2)$.

Increasing the stator phase number leads to more phase cancellation of the low order harmonic components. Figure 4.7 shows the FFT plot of the harmonic components in the output dc voltage normalised by the phase ac voltage amplitude. Its clear that only even harmonics exist and the lowest dominant harmonics on the output voltage are shifted to higher frequencies where their amplitudes diminish inversely with the number of stator phases. This desirable attribute eases the requirement for passive

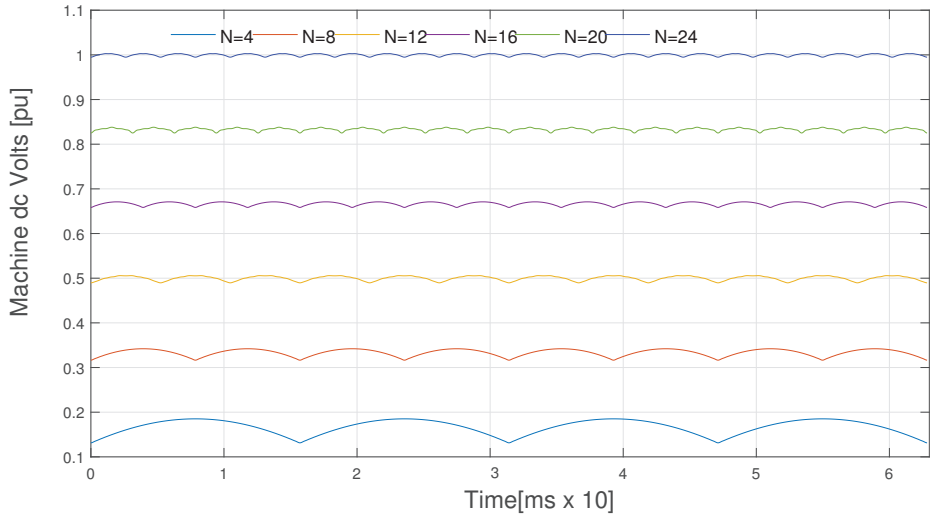

Fig. 4.6 Normalised Machine DC link voltage variation for increasing Stator Phase Number.

filters on the generator output, consequently smaller or no passive filter components will be required if the stator phase number is sufficiently high.

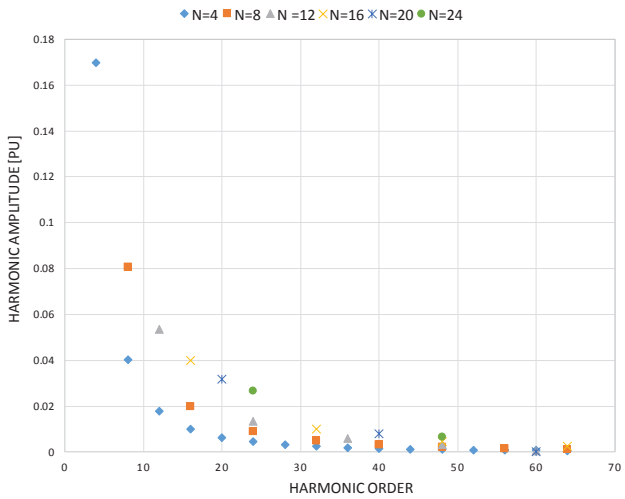

Fig. 4.7 DC Link Voltage Harmonics Variation with Increasing Machine Stator Phase Number (N)

Performing a similar analysis on the dc link current and ac phase current show similar harmonic cancelation behaviour to that of the dc link voltage. For this current source drive topology, the dominant lowest ripple current harmonic order is influenced by the number of stator phases. The dc link current is dependent on the load impedance

and can be expressed as;

$$I_{dc}(\theta_i) = \frac{V_{dc_N}(\theta_i)}{Z_{load}} \tag{4.13}$$

where $V_{dc_N}(\theta_i)$ is defined by (4.12) and Z_{load} is the circuit equivalent load impedance. The equivalent circuit load impedance will comprise of the machine reactance, dc link filter reactance and an equivalent impedance determined by the load characteristics. From (4.6) an expression of the ac phase current $I_{ac}(\theta_i)$ can be obtained by substituting (4.13) to give;

$$I_{ac}(\theta_i) = \frac{V_{dc_N}(\theta_i)}{Z_{load}} S(\theta_i) \tag{4.14}$$

where $S(\theta_i)$ is defined by (4.8).

If the number of stator phases is sufficiently increased, a small dc link current ripple filtering inductor will be required. The dc link inductor can be sized to reduce the amplitude of the lowest ripple harmonic order to have negligible detrimental effect on the machine performance. In such a case, the machine phase current can be considered to be a constant dc current except for the commutation intervals when the phase current reverses polarity. As highlighted earlier, the commutating inductance and machine voltages influence the rate at which current commutation occurs. Assuming linear current commutation, then the ac phase current waveform can simply be represented by a trapezoidal waveform Fourier expression;

$$I_{ac}(\theta_i) = I_{dc} \sum_{k=1}^{\infty} \cos(k(\theta_i - \pi(0.5 - \tau_\mu))) \frac{\sin(k\pi/2)}{k\pi/2} \frac{\sin(k\pi\tau_\mu)}{k\pi\tau_\mu} \tag{4.15}$$

where only odd harmonics exist, τ_μ is the ratio of the commutation overlap time (t_μ) to the fundamental period (T) i.e. $\tau_\mu = t_\mu / T$. The commutation overlap time can be readily derived from the expression of the commutation overlap angle equation (4.1) for a given operating machine frequency. Analysis of the above waveform shows that the commutation overlap reduces any ac harmonic current component in a ratio of approximately $\frac{\sin(k\pi\tau_\mu)}{k\pi\tau_\mu}$. From (4.15) above, the impact of the commutating inductance on the fundamental rms value of the phase current I_{ac_1} can be expressed as;

$$I_{ac_1} = \frac{2I_{dc}}{\pi\sqrt{2}} [\frac{\sin(\pi\tau_\mu)}{\pi\tau_\mu}] \tag{4.16}$$

When the commutating inductance approaches zero, the rms fundamental component of the machine phase current approaches;

$$I_{ac_1} = \frac{2I_{dc}}{\pi\sqrt{2}} \tag{4.17}$$

operation, only positive dc voltage, reversal of dc voltage not possible.

4.4.4 Passive Commutator Topology Drawbacks

The passive commutator topology allows only one quadrant operation, i.e. only unidirectional positive dc link voltage and current is possible. As such this topology only applies to generator applications. A significant drawback of this passive H-bridge commutator topology is its inability to control the rectified dc voltage output and consequent inability to limit potential fault currents via the commutator H-bridge power electronic devices. The peak per phase short circuit current I_{sc} can be expressed as;

$$I_{sc} = \frac{V_{ph}}{\omega L_{sc}} \tag{4.18}$$

where V_{ph} is the machine phase voltage, V_{ph} is the machine angular frequency and L_{sc} is the generator phase short circuit inductance.

To protect the machine from module faults, fuses can be used between the generator phase winding and power modules. Fuses could also protect the modules from insulation faults in the coils if the voltage rating is high enough. In the event of an H-bridge module failure the coils would still be subjected to a high short circuit current until the fuse blows. The generator can be designed to handle the mechanical stress induced by the phase short circuit as it would be low compared with the total machine torque. A transient voltage suppressor would be required across the coils to absorb the energy stored in the coil inductance when the fuse blows.

The inherent inability to control the machine's generated output dc link voltage via the H-bridge power electronic modules can potentially limit the range of applications particulary where constant dc link voltage operation is required. This drawback can be alleviated or in some cases eliminated by some system design choices such as the

choice of generating machine excitation system or the choice of prime mover coupled to the generating machine as will be highlighted in the possible control schemes below.

4.4.5 Passive Commutator Topology Control Schemes

The passive commutator topology discussed above has limited degrees of freedom in terms of control variables. For designs that employ machines with would rotors, only two degrees of freedom exist either via prime mover speed control or machine field current excitation control. The generator output dc link voltage can be controlled by controlling the voltage applied to the field winding terminals of the generating unit. If a wide dc link voltage operating range is required, field excitation control will impose limitations on the operating range owing to the field weakening effect which can curtail the generator's torque capability if lower dc link voltages are required at significant loads. The field excitation control strategy would suite applications where the load profiles increase with increasing dc link voltages or constant dc applications. Obviously the dc link voltage control bandwidth is constrained by the machine's rotor time constant and the voltage forcing capability of the field converter.

Figure 4.8 shows an example of this passive commutator generator topology connected to feed power to the ac grid. In this figure two current source converters connected in series are employed for grid connection. This control scheme employs the machine field excitation control to regulate the generator output dc link voltage. Each of the machine commutator H-bridges comprise of diodes as the commutator power electronic devices. The H-bridges are connected to form two parallel current paths, each with several H-bridges connected in series. A small dc link inductor is connected to decouple the machine from the ac network converter.

In this control strategy, a lower bandwidth outer dc voltage controller regulates the dc link voltage and generates a field current reference for a higher bandwidth inner control loop that regulates the machine flux, hence terminal voltage via excitation field current. The network converter regulates the generator current, ac active and reactive power fed to the grid as depicted in figure 4.8.

Similar to typical LCI drive control schemes [27], the dc link current and consequently machine torque & generated power are controlled by the network converter.

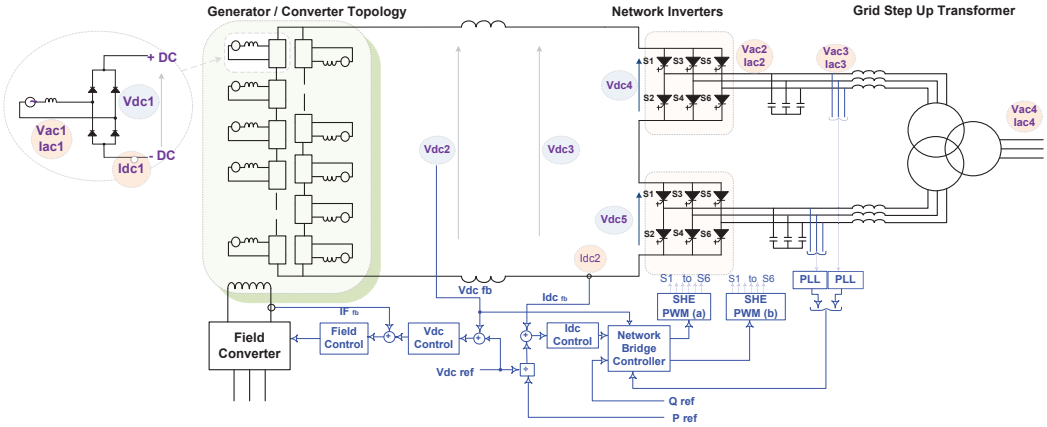

Fig. 4.8 Schematic of Passive Commutator Generator Topology Control Scheme

An inherent advantage of this current source topology in comparison to the voltage source converter generator topologies is that the generator can continue to generate and feed power to the grid even when the output dc link voltage is much lower that the peak grid ac voltage. Conversely, to ensure dc current control is maintained, the generator average output dc link voltage should not exceed the network converter ac voltage. This can be readily observed from the relationship between the network and dc link voltages and currents given in (4.19) and (4.20). The voltage and current relationships between the network bridge output and dc link can be defined as;

$$V_{dc} = mV_{ac}\cos(\varphi) \tag{4.19}$$

$$I_{ac} = mI_{dc} \tag{4.20}$$

where, V_{dc} and I_{dc} are the average dc voltage and current, $\cos(\varphi)$ specified the desired operating power factor. The modulation (m) ranges from $0 \leq m < 1$. Its clear from (4.19) that for the constrained range of m, the rectified generator output dc link voltage should not exceed the peak of the ac network voltage if control of the dc link current is to be retained. Since the network bridges controls the machine current in this passive commutator topology, the network converter bridges can be used to rapidly shut down the drive in the event of faults.

To improve the overall efficiency of the generating system, the grid converter efficiency can be improved by interleaving the network converter bridges. Interleaving

PWM facilitates a reduction in PWM switching frequency by exploiting its harmonic phase cancellation attribute. For higher generator output voltages, more network converter bridges can be seriesed and connected to the ac grid via a multiple secondary winding transformer. This series connection of the network bridges also avoids current circulation issues that can be experienced in topologies such as parallel connected network converters presented in [105]. The use of two series connected Current Source Inverters (CSI) in medium voltage applications has been described in [108] and [109].

4.4.6 Selective Harmonic Elimination

The network bridge converter efficiency can be improved even further by employing PWM modulation techniques that minimises switching frequency such as Selective Harmonic Elimination (SHE) strategy presented in [110–112]. Usually low order current harmonics have a higher priority to be eliminated owing to their undesirable detrimental impact on the electrical system. Using SHE PWM, resonance phenomena can be effectively suppressed. The switching angles in the modulated rectifier are selected in such a way that the harmonics in PWM current waveform, which may excite any resonance, are selectively eliminated whilst using the lowest switching frequency possible.

The underlying principle of SHE PWM is that the fundamental and harmonic amplitudes of a symmetrical PWM waveform are non linear functions of the number of switching angles in the first quarter fundamental period. Setting the fundamental amplitude to a desired pre-specified value and the other low order harmonics to zero results in a system of non linear equations that can be iteratively solved using numerical methods such as Newton Raphson method. Due to the high complexity solving harmonic elimination equations on-line during real time operation, the equations can be solved off-line and results (notch angles) stored in a look-up table. The angles can then be retrieved from the look-up table and the pulse widths are then generated for a given PWM modulation reference. Unlike the phase controlled series connected network bridges presented in [113] which require an additional converter to filter harmonics, SHE PWM network converters operating at low switching frequencies can be employed to give low ac harmonics due to SHE PWM's superior harmonic

performance. This PWM modulation strategy and its implementation will be discussed in detail later in the control system implementation chapter 8.

4.4.7 Case Study: Simulated Operation of Passive Commutator Topology

The topology concept depicted in figure 4.8 has been completely implemented and assessed in the Matlab- Simulink & PLECS environment along with the proposed control system. The topology using diode H-bridge phase commutator configuration with a 24 phase machine has been simulated to assess its dynamic and steady state operating characteristics. The simulation assumed the following prototype machine parameters:

1. Machine:
    - Rated Power = 600 kW
    - Stator Phases = 24 $phases$
    - Rated Speed = 100 rpm
    - Machine Poles = 4 $pole$
    - Commutating Inductance = 6 mH
    - Rated phase Voltage = 160 $Vrms$
2. DC Link:
    - DC Inductance = 0.5 mH
    - Rated DC Volts = 1500 V
    - Rated DC Current = 400 A
3. AC Network
    - Transformer vector group = $Yy0$
    - AC Primary Line Volts = 3460 V
    - AC Secondary Volts = 690 V
    - AC Transformer Impedance = 5 %
    - AC Frequency = 50 Hz
    - Grid Impedance = 20 %

The simulated machine/converter topology circuit has two parallel paths ($\gamma = 2$), each with 12 H-bridge phase modules connected in series. Two network bridges are

series connected three-phase bridges employing fully controllable switches with bidirectional voltage blocking capability with unidirectional current conduction capability. SHE PWM scheme was implemented for the network bridges to control the dc link current. The network bridges use phase locked loops to synchronise the PWM current switching events to the ac network angular frequency to ensure correct active and reactive power injection into the ac grid. A three-phase capacitor filter is required on the ac side of the network bridge of the CSI to assist current commutation and filter harmonic components.

Simulated Machine H-bridge Waveforms

Figure 4.9 shows the per unit ac machine phase voltages and currents for two adjacent single phase diode H-bridge commutator modules. For this 24 phase machine, each ac phase current and voltage waveform is phase displaced by $(2\pi/24)$ radians from the adjacent phase. It can be seen that the high stator phase number and a small dc link inductance has resulted in negligible dc link current ripple. As highlighted in earlier discussion, the ac phase current is a trapezoidal waveform with negligible ripple current at 24 times the fundamental frequency. Ignoring the 24^{th} ripple harmonic component, it can also be observed that the phase current is predominantly dc with an amplitude of half the total machine output dc link current except for the brief periods when the phase is undergoing current commutation and phase current reversal. The duration of the current commutation is mainly dictated by the machine commutating inductance and the phase back emf as highlighted by (4.1).

Simulated DC Link Waveforms

Figure 4.10 shows the output dc link voltages of the two adjacent H-bridge phase modules and the overall machine dc output voltage and current scaled to the same per unit base. The individual phase rectified dc link voltage is a small fraction of the total machine dc link voltage and the corresponding H-bridges dc link current is half of the total machine dc link voltage. In comparison to the H-bridge waveforms in figure 4.5, owing to the network CSR PWM switching, the generator output dc link voltage has a noticeable superimposed modulated PWM dc voltage component. This is also noticed

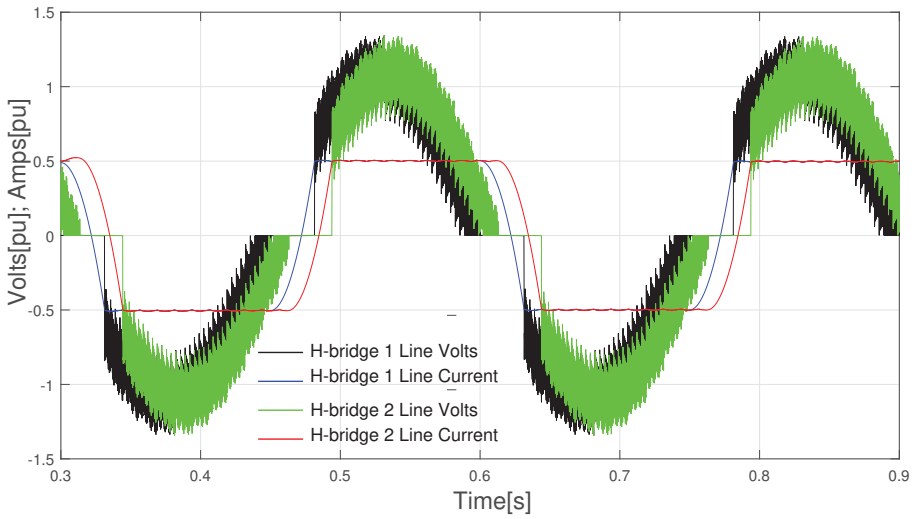

Fig. 4.9 Waveforms of Two Adjacent H-bridges Phase Voltages & Phase Currents

on the machine phase terminal voltages of figure 4.9. This PWM voltage component is at a much higher frequency compared to the machine fundamental and results in negligible high frequency current component as seen from the dc link current and consequently has no detrimental effect on the operation of the drive.

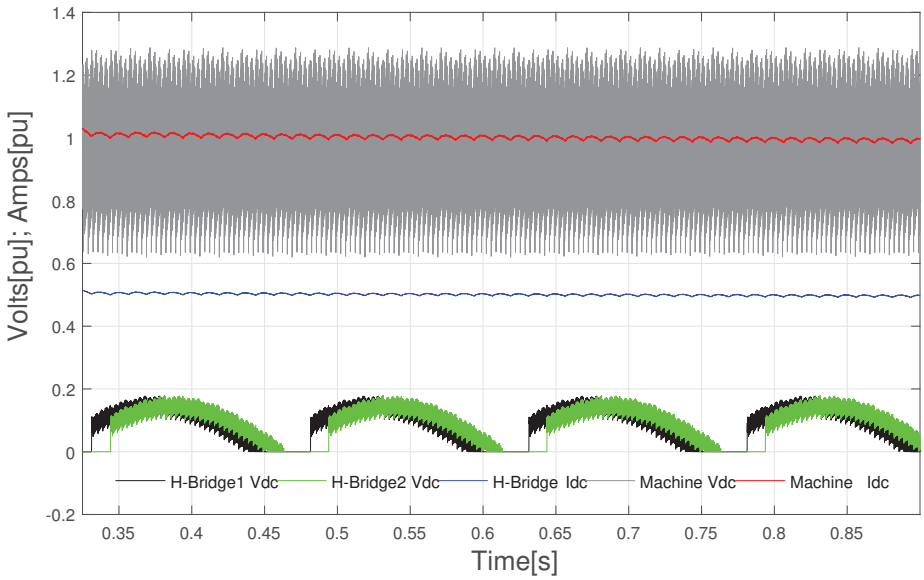

Fig. 4.10 Waveforms of Output dc Voltages of Two Adjacent H-bridge Phase Modules, H-bridge dc Current and Machine dc Current & Voltage.

Simulated Network Bridge Waveforms

The network converter bridges are controlled to regulate the active and reactive power exported to the ac grid. SHE PWM with 7 chopping angles was implemented on each of the two series connected bridges to eliminate 5^{th},7^{th},11^{th},13^{th},17^{th} and 19^{th}harmonics from each bridge's ac line currents. Figure 4.11 shows the simulated network converter bridge output ac three phase ac currents measured after the input filter terminal and directly on the converter bridge output before the input filter. As can be seen in these ac currents, the two network converter bridges have been interleaved by 7.5^{o} to achieve harmonic phase cancelation on the primary side of the transformer.

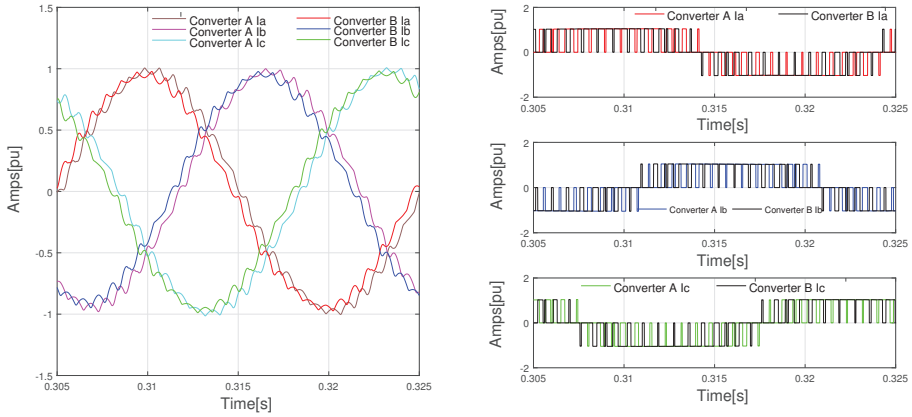

Fig. 4.11 Network Converter Bridges Line currents; (a) Measured After the Input Filter and (b) Measured at Converter Output Current

Figure 4.12 shows a single network bridge voltage on the transformer secondary and the corresponding phase currents. The phase voltage and corresponding phase current are completely out of phase with each other, indicating unit power factor generating mode of the network converter.

Simulated Network Grid Connection Waveforms

Figure 4.13 shows the transformer primary voltage and current waveforms. As can be seen they are almost sinusoidal in comparison to the transformer winding secondary voltages and current waveforms of figure 4.12.

Figure 4.14 and figure 4.15 shows the FFT plots of the transformer primary and secondary ac voltage and current waveforms which shows very low harmonic content

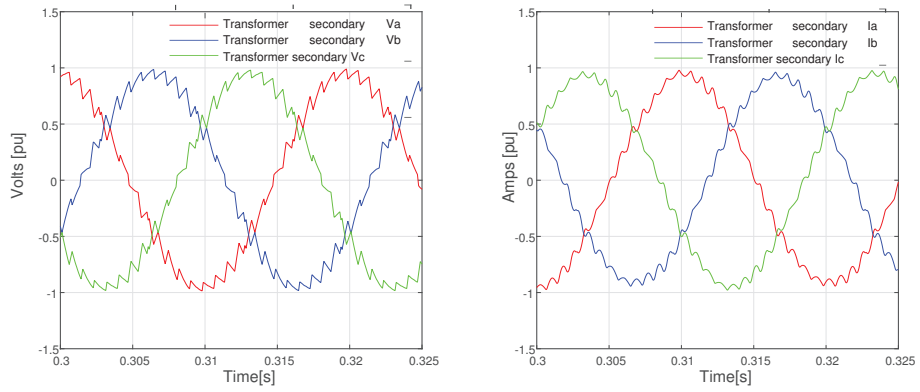

Fig. 4.12 Single Network Converter Input Phase Voltages and Currents at the Transformer Secondary Winding

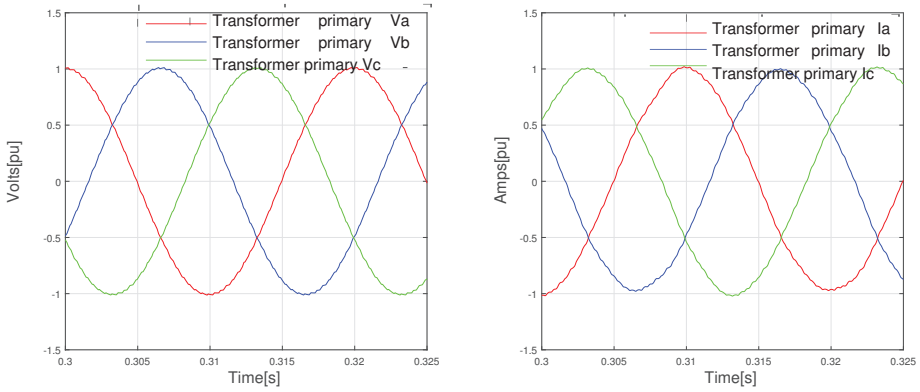

Fig. 4.13 Transformer Primary; (a) Phase Voltages and (b) Phase Currents

produced by the interleaved SHE PWM network bridges on the transformer primary side ac grid point of common coupling. As can be seen, despite the individual network converter's output voltage and current total harmonic distortion being 5.95% and 4.63% respectively, the total harmonic distortion at the transformer primary side of less than 0.64% and 1.54% is achieved for the voltages and currents respectively.

For the SHE PWM scheme, the first non eliminated low order harmonic in the ac phase voltages and currents is the 23^{rd} harmonic of the fundamental component. The SHE PWM implemented with 7 chopping angles successfully eliminates the 5^{th}, 7^{th}, 11^{th}, 17^{th}, and 19^{th} harmonics from the ac voltage and current waveforms. Owing to three phase symmetry and high zero sequence impedance, triplen harmonics do not exist in this topology.

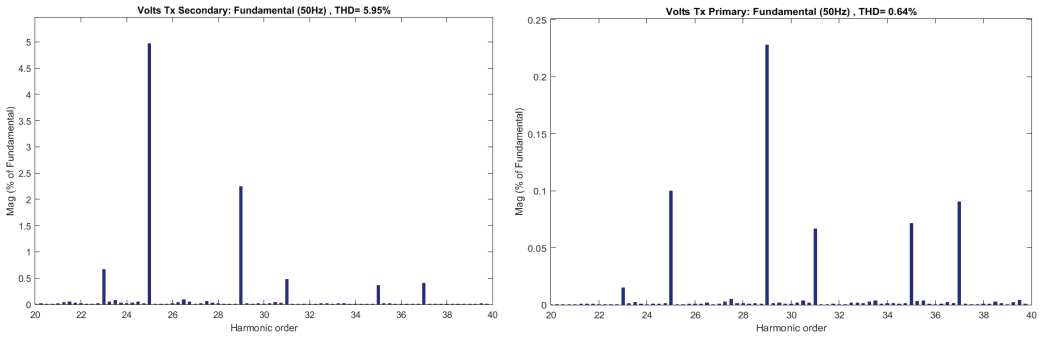

Fig. 4.14 FFT of Transformer Phase Currents (a) Secondary Side and (b) Primary Side

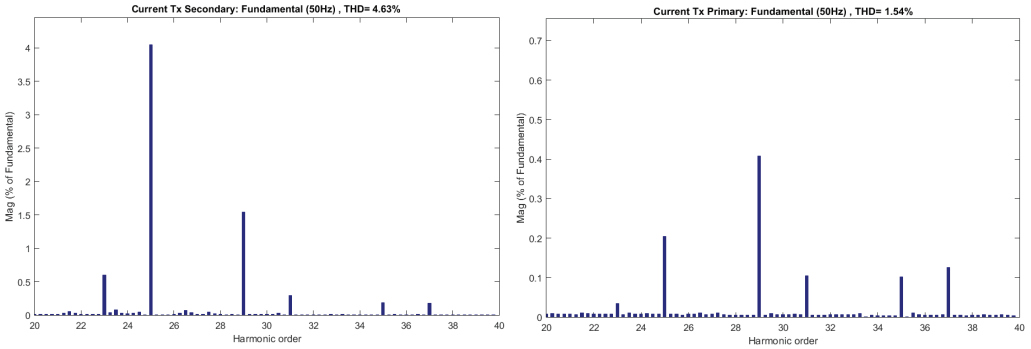

Fig. 4.15 FFT of Transformer Phase Voltages (a) Secondary Side, (b)Primary Side Waveforms

Simulated Drive Power Control Waveforms

To access the ability of this topology to control the generated power fed to the ac grid, the simulation was conducted assuming a worst case scenario where there is no means of controlling the machine output dc link voltage. Instead, only the dc link current and ac active and reactive power were controlled by the network bridges, assuming constant generating machine speed and airgap flux. Figure 4.16 (a) shows the dc link current reference and feedback signals when the dc current reference is ramped from zero to 1.0 pu and then down to 0.3 pu. As can be seen, the network bridges can accurately control the current to follow a defined reference signal. Figure 4.16 (b) shows the corresponding machine phase winding ac voltage and current waveforms. Figure 4.16 (c) shows the machine output dc power and active power exported to the ac grid from this passive commutator multilevel 24 phase machine. Figure 4.16 (d) shows the corresponding single machine phase H-bridge output dc link voltage & current and the associated machine total dc link voltage and current waveforms.

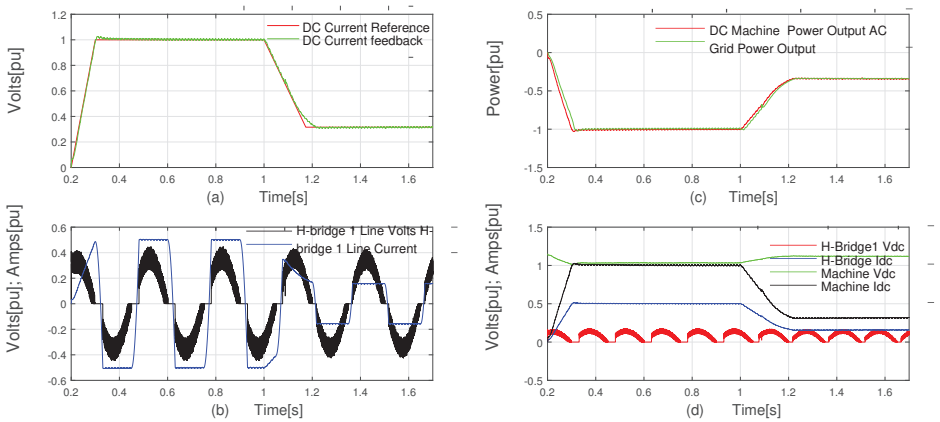

Fig. 4.16 Passive Generator DC Current and Output Power Control Waveforms

Discussion

The above simulation has demonstrated the feasibility of the passive commutator multiphase multilevel topology to act as a generator with the ability to control the generated power exported to the ac grid and also meet the typical ac harmonic and total harmonic distortion requirements. The attractive features of this topology are; its simplicity, the use of robust diode commutator power electronic devices that do not require complex gating electronics & control schemes. These features can consequently lead to very high reliability dc generators which requires very little or no regular maintenance. Such generator can be deployed in remote or harsh environments which are not readily accessible. If desirable, the network converters can be located in easily accessible locations away from the generating machine via dc cable connections. The cable impedance can act to filter harmonics and also reduce or eliminate the need for dc link inductance if their equivalent ac impedance is sufficiently high.

For a given machine output dc voltage, the higher the machine phase number, the lower the voltage rating of individual H-bridge cells. Thus, if the machine phase number is sufficiently increased high output dc voltages can be realised with Commercially Off The Shelf (COTS) low voltage semiconductor devices. With this simple passive commutator multilevel multiphase topology, machine and passive commutators capable of generating high dc link voltages can be realised. For example, 15kV dc output voltage can be readily realised by machine with 48 stator phase windings with a rated phase voltage of 695 Vrms. The passive diode commutator can be designed using

COTS diodes without the need for series diode connections in the phase H-bridge arms. The required maximum surge peak forward and reverse blocking voltage V_{DSM} for the diodes is given by (4.21) as;

$$V_{DSM} = \sqrt{2} V_{s_{rms}} \kappa \tag{4.21}$$

where $V_{s_{rms}}$ is the rms phase voltage, κ is a safety factor, $\kappa = 2.5$ being typical for rectifier applications [114]. In this case commercially available diodes rated at 2.4 kV can be used. The modularity of the phase H-bridge topology will facilitate manufacturing, installation and repair of the commutator.

4.5 Active Commutator Topology Analysis

The inability of the passive electronic commutator topology discussed above to actively control the dc link voltage and also its failure to interrupt machine fault currents via the machine's electronic commutator make this topology unattractive for certain applications such as motoring drives where machine output dc voltage control and rapid current interruption via machine electronic commutator requirements are paramount. Additionally, for applications that require two quadrant machine operation in both motoring and generating modes, the passive topology can not be used. This section extends the multilevel multiphase concept to electronic commutators with actively controlled power electronic switching devices. For purposes of analysing the active topologies, the active commutator topologies will be split into two distinct groups. The first group comprises of active commutators that only permit one quadrant generator operation similar to the passive topologies. The second group comprises of active commutators that also permit inversion, i.e. both motoring and generating two quadrant operation. The operating quadrants for the proposed topologies are highlighted in figure 4.17 showing the polarity of the dc link voltage and current for the entire 4 quadrant torque speed range.

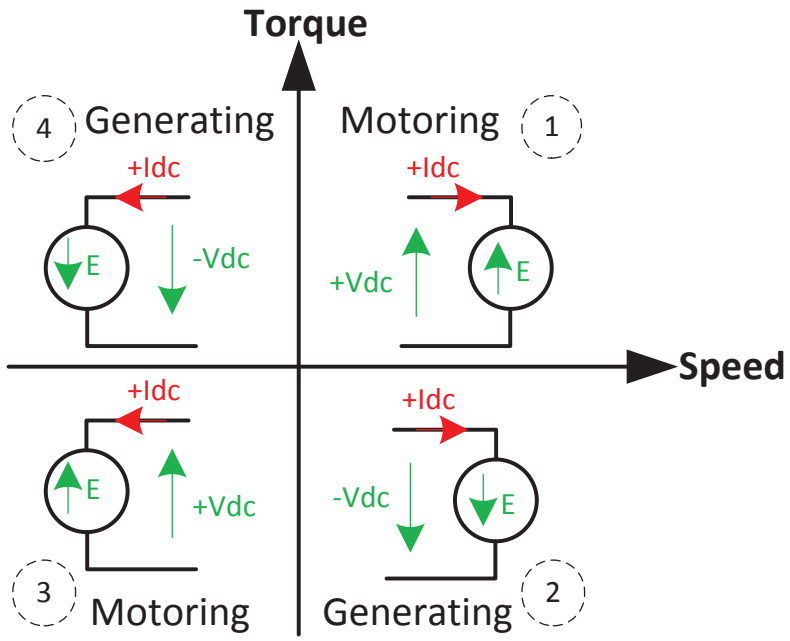

Fig. 4.17 Machine & Converter Topology: Four Quadrants of Operation

4.5.1 Single Quadrant Active Commutator

Topologies that enable machines with high output dc link voltages without the need for series connection of several devices per phase arm have been reported in [115–118] for wind generator applications. This approach focused on series connection of rectifier outputs of several conventional three phase generating machines. This approach poses some control challenges in applications where high dynamic performance is required since the control of several machines has to be accurately coordinated. Another drawback of this approach is the additional penalty incurred on the required interconnections, both in terms of control and power cable runs required between the series connected generators for successful synchronised operation.

In this work, owing to the high stator phase number, high machine output dc link voltage output is achievable on a single machine, thereby avoiding the need of series connected several machine dc outputs. The single quadrant active commutator topology features multiphase machine & active commutator topologies that work

in generating mode only with the ability to control the machine's generated output dc voltage and capability of interrupting fault currents via the active commutator circuits. The topology configuration is similar to that of the passive commutator presented earlier. However, the multilevel single phase H-bridge commutator cells employ a combination of gate triggered power electronic switching devices and diodes. Single phase H-bridge topologies that operate in this mode are widely documented [119–122] *et-al*. Their operational behaviour will be briefly examined to expose their performance characteristics when applied to the multiphase multilevel machine commutator topologies presented in this work.

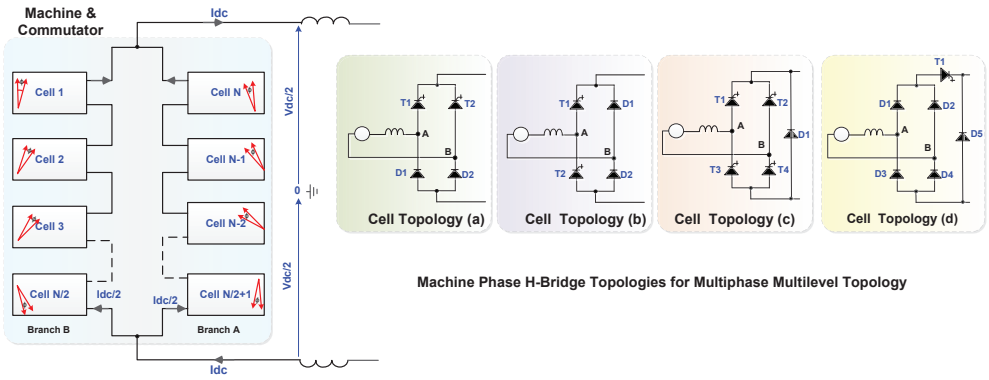

Fig. 4.18 Multilevel Machine Phase H-Bridge Cell Topologies for Half Controlled Commutators

Figure 4.18 shows the possible H-bridge cell topologies applicable to this single quadrant topology. Despite having fewer gate triggered power electronic devices, these topologies provide output dc link voltage control over the entire rectifier operating range. The H-bridge circuit depicted in figure 4.18 (a) with gate triggered devices in the top arms and diodes in the bottom arms of the H-bridge is a half controlled topology. It can be considered as two separate series connected commutating groups, one with a variable delay angle α and the other with a permanent delay angle of zero. One advantage of this circuit is that since the controlled power electronic devices are connect to the same potential, simple gating circuitry which do not require galvanic isolation techniques such as pulse transformers can be employed.

Circuits depicted in figure 4.18 (b), (c) and (d) contain inbuilt free wheeling paths not possessed by the topology depicted in (a). In cases where the machine H-bridge

instantaneous output dc voltage is always positive such as at very small values of α and very small commutating inductances, the freewheeling diode will have no effect. For larger α and large machine commutating inductances, the freewheeling diode prevents negative instantaneous output voltages by conducting the dc current that would otherwise go trough the machine phase winding. As a consequence, such topologies consume less reactive power since the dc link current flows through this freewheeling path during machine current commutation. Another advantage of the freewheeling diode is that in the event of machine or commutator H-bridge phase arm device circuit faults, there is still a path for the load current via this freewheeling diode. As a result, the overvoltage suppression circuitry required has to be rated for the machine phase circuit only, with a much lower ratio of inductive to resistive impedance (*X/R*) ratio compared to that which includes the load inductances. The lower the *X/R* ratio of a circuit, the lower the peak short circuit current & the shorter the dc component will take to decay i.e. shorter time constant. Additionally, all these half controlled H-bridges machine converter cells in this topology can simply be turned off by pulse inhibiting the controlled H-bridge devices to effectively disconnect the machine phase(s)from the rest of the load circuitry.

The half controlled H-bridge can be conveniently analysed by splitting it into; one uncontrolled half bridge and one controlled half bridge. The uncontrolled half bridge produces a fixed output dc voltage relative to the machine phase ac neutral point equal to;

$$V_{dc_a} = 0.5V_{ac}\frac{\sin(\pi/2)}{\pi/2} - \frac{I_{dc}L_c\omega}{2\pi} \tag{4.22}$$

The controlled half produces an output dc voltage dependent on the firing delay angle α given by;

$$V_{dc_b} = 0.5V_{ac}\cos(\alpha)\frac{\sin(\pi/2)}{\pi/2} - \frac{I_{dc}L_c\omega}{2\pi} \tag{4.23}$$

The total mean output dc link voltage is given by the sum of V_{dc_a} and V_{dc_b} as;

$$V_{dc} = 0.5V_{ac}\frac{\sin(\pi/2)}{\pi/2}(1+\cos(\alpha)) - \frac{I_{dc}L_c\omega}{\pi} = \frac{V_{ac}}{\pi}(1+\cos(\alpha)) - \frac{I_{dc}L_c\omega}{\pi} \tag{4.24}$$

The firing delay angle control range is bound between $0 \leq \alpha \leq \pi$. From this resultant dc voltage expression, its clear that no inversion is possible as the voltage can not be negative for this α control range. As such this limits the operating quadrants to the generating mode only. Inspection of (4.2) of the passive topology and (4.24) shows that the commutating inductance effect on output voltage regulation is independent of phase control for natural phase current commutation. Closer analysis of the operation of the half bridge circuit topologies given in figure 4.18 (a), (b) and (c) also show that these circuits exhibit the same electrical functional behaviour. The output dc voltage and ac phase line current waveforms of H-bridge topologies (a),(b) and (c) are similar. Although topology (d) has the advantage that it contains a single gate controlled switch which is phase controlled to regulate the output dc link voltage, it cannot regulate dc link voltage above a given minimum dc link current threshold if switching devices such as Thyristors with no forced gate turn off capability is used owing to the device current remaining above the Thyristor holding current. Therefore, only topologies (a), (b) and (c) are considered applicable to this current source machine/converter topology if switching devices used have no forced current turn off capability. Topology (d) is however applicable if switching devices with forced current turn off capability such as Gate Turn Off Thyristor (GTO) are employed.

Carrying out Fourier analysis for the output ripple voltage on these half controlled topologies give an expression of the total k^{th} output ripple harmonic voltage on the dc link as;

$$V_k = \frac{V_{ac}}{\pi(k^2-1)} \cos(k\pi/2)\{k\sin(\alpha)\sin(k(\omega t+\varphi)) - \cos(\alpha)\cos(k(\omega t+\varphi)) - \cos(k(\omega t+\varphi+\alpha))\} \tag{4.25}$$

where; φ is the machine winding phase displacement given by $\varphi = 2\pi/N$ for a machine with N stator phases.

Owing to the $\cos(k\pi/2)$ term in (4.25), only even harmonics exist on the output dc link voltage. Its clear from inspection of the above equation that the firing angle α affects the harmonic voltage ripple amplitude. The variation of firing angle with individual ripple harmonics of the half controlled bridge topology is depicted graphically in figure 4.19 when normalised by the maximum H-bridge dc voltage.

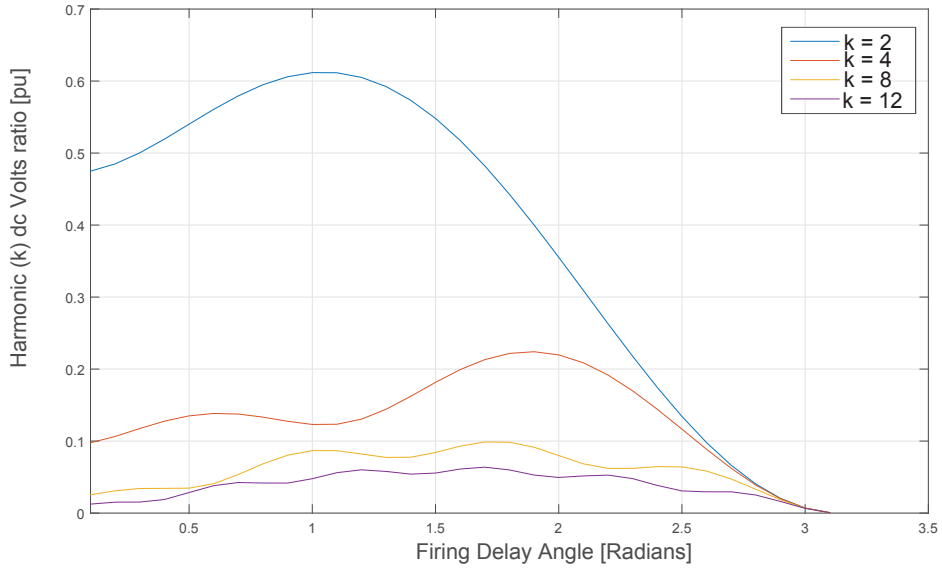

Fig. 4.19 Variation of H-bridge Output DC Individual Harmonic (k) with Firing Angle

When applied individually to rectifier circuits, the half controlled H- bridge topology suffers from the high output voltage ripple content, dominated by the second harmonic as shown above. However, as has been seen in the previous analysis, when several bridges are connected in series and fed from phase shifted ac sources, the dominant low order harmonics diminish due to phase cancellation. Such is the case with multiphase multilevel topology presented in this work. With series connection of the H-bridge cells, the dc current I_{dc} is common to all seriesed machine phase H-bridge commutator cells.

The average dc link voltage of each machine phase H-bridge is given by (4.24). The resultant average dc link voltage for a machine with N stator phases is thus given by simple summation of the series connected H-bridge output voltages to give;

$$V_{dc} = V_{dc_1} + V_{dc_2} + \cdots + V_{dc_{N/2}} = \frac{V_{ac}}{\pi}\left(N/2 + \cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_{N/2})\right) - \frac{NI_{dc}L_c\omega}{2\pi} \tag{4.26}$$

In the general case all seriesed H-bridges are controlled to have the same firing angle, i.e. $\alpha_1 = \alpha_2 \cdots = \alpha$. Thus, the average dc voltage becomes;

$$V_{dc} = \frac{NV_{ac}}{2\pi}\left(1 + \cos(\alpha) - I_{dc}L_c\omega\right) \tag{4.27}$$

The machine phase current is common to all seriesed H-bridges and for a machine with two paralleled commutator circuits, and equals half the total dc link current for symmetrical machine operation. The machine's total output dc link power can thus be computed as the product of the total dc link voltage and dc link current as;

$$P_{dc} = \frac{NV_{ac}I_{dc}}{2\pi}\left(1+\cos(\alpha)-I_{dc}L_c\omega\right) \tag{4.28}$$

Topology Operation

The operation of the half controlled H-bridge topology is simple. With reference to figure 4.18, using topology (b) as an example, device T1 is triggered α degrees after the voltage at ac terminal A has gone positive relative to terminal B and conducts current with diode D2. When the machine phase terminal B voltage becomes positive, the phase current will start to naturally commutate to D1 and eventually reaches zero. At this point the entire load current from adjacent seriesed bridges is conducted by the two freewheeling diodes D1 & D2. This is also depicted in the simulated waveforms of the this topology as shown in figure 4.20. Its clear from figure 4.20 (b) and (d) that the machine phase does not carry any current between $t = 0.31s$ to $t = 0.35$, only the freewheeling diodes of the phase H-bridge carry load current. The machine phase current stays at zero during this machine phase open circuit condition until the device T2 is triggered α degrees after terminal B voltage has gone positive relative to terminal A. At this point the load current starts to commutate from D2 to T2 and the phase current rapidly builds up to half the total machine dc link current. Topology (a) is controlled in a similar manner to topology (b) except that either device T1 or T2 must remain in a conducting state to carry the load current during the commutation intervals. A disadvantage of topology (a) which is not possible in topology (b), (c) and (d) is the possibility of half-waving that can occur in the event of commutation failure.

Control of topology (c) is similar to that above except that the device pairs (T1, T4) and (T2, T3) are triggered in a similar fashion to topology (b) and the H-bridge cells and machine waveforms are identical to those in figure 4.20, with the exception of the freewheeling diode waveforms. The freewheeling diode in topology (c) allows natural freewheeling of the load current and conduct load current in the interval t_1 from $t = 0$ to $t = \alpha/\omega$ for both half cycles. The freewheeling diode current is zero for the rest of

the fundamental cycle. The peak current of the diode is the same as the peak phase current but its average current is much lower. If the effect of commutating inductance is negligible, the freewheeling diode average current is given by;

$$I_{D_1} = \frac{I_{dc}}{2}\left[\frac{t_1}{T/2}\right] = \frac{I_{dc}}{2}\frac{\alpha}{\pi} \tag{4.29}$$

where, T if the fundamental period. If the diode is not required for purposes of permanently bypassing the H-bridge over the fundamental cycle, then its current and thermal rating is only a fraction of the H-bridge arm devices rating.

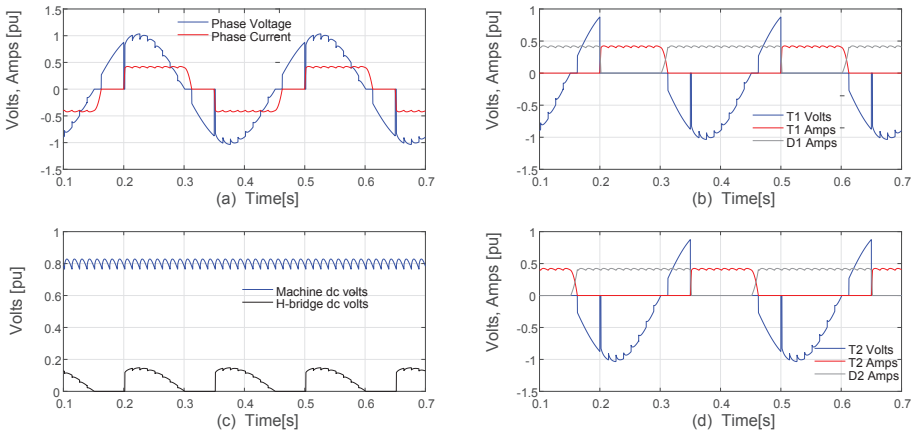

Fig. 4.20 24 Phase Multilevel topology; Machine Phase H-bridge Topology (b) Waveforms with $\alpha = 60$ degrees.

Figure 4.20 shows the simulated waveforms of a 24 phase machine with two paralleled commutator circuits, each comprising of 12 H-bridge phase cells connected in series employing half bridge topology (b). Figure 4.20 (a) shows a single machine phase voltage and current waveforms when operating at a firing angle of 60 degrees. Figure 4.20 (b) & (d) show H-bridge devices (T1, D1) & (T2, D2) voltage and current waveforms respectively. The total machine output dc link voltage and also a single H-bridge dc link voltage waveforms are shown in figure 4.20 (c). Analysis of this topology shows that the machine output dc link voltage can be controlled throughout the entire positive quadrant (generator mode only) voltage range via individual H-bridge phase control from $\frac{2V_{ac}}{\pi}$ to 0 volts, for firing angle range $0 \leq \alpha \leq \pi$. For a given stator frequency, the achievable control bandwidth of the dc link voltage control increases with increasing machine stator phase number owing to the corresponding

reduction in machine H-bridge phase triggering interval period governed by the phase shift φ which varies inversely with machine phase number.

Machine Current Sharing

Since this multilevel topology feature at least two parallel branches of machine commutator circuits, each with several series connected H-bridge cells, its possible for the paralleled machine circuits not to evenly share the dc link current. Current mis-share can occur due to a variety of reasons such as, machine and converter manufacturing tolerances or environmental conditions which can result in unsymmetrical impedances in the paralleled circuits or finite tolerance in the H-bridge cells synchronisation or device triggering circuits. Ultimately, this can result in one part of the paralleled circuits conducting a bigger share of the dc current than the other. As such, if special provisions are not made to address the current mis-share, it can lead to increased current and thermal stresses of the machine phase windings and associated H-bridge circuits that shoulder the higher current and ultimately negatively impact the drive system reliability [123–125].

Proposed Current Balancing Strategy. In order to significantly curtail or better still eliminate current mis-share, either additional hardware or control measures have to be formulated and implemented for these multiphase multilevel topologies. Hardware measures are least favourable as they add cost and footprint to the overall machine and converter drive unit and will not be explored further. Control measures are therefore preferred as their impact on cost and footprint is insignificant in comparison to hardware based current balancing strategies. Several current balancing techniques between paralleled converters have been reported [126–128, 125]. An overview and comparison of current balancing strategies for paralleled converters have been presented in [129] and grouped into two distinct methods, namely, droop based methods and active current sharing based methods. In this work, droop based methods have been discounted owing to their open loop nature and adverse impact on output voltage regulation required to achieve the droop characteristics. Instead an active current sharing control strategy is proposed. The goal of the proposed scheme is to ensure that equal rms ac current exists in the paralleled machine branches. It can be shown that

the machine fundamental phase rms current is given by;

$$I_{ac} = \frac{I_{dc}}{2}\sqrt{\left[1 - \frac{\alpha}{\pi}\right]} \tag{4.30}$$

Inspection of (4.30) shows that the rms phase commutator H-bridge current can be selectively influenced by the firing angle α. In the proposed scheme, rather than trying to control the current mis-share on an individual phase module by phase module basis, it is possible and more effective to achieve current sharing by actively controlling the relative phase shift between the paralleled machine circuits, bearing in mind that all seriesed phase H-bridge modules in a branch carry the same phase current. Another attractive feature of this proposed scheme is that it naturally yields interleaving characteristics between the paralleled branches of machine phases, leading to the possibility of further reduction in machine torque ripple and output dc link voltage ripple.

In this proposed scheme, a global dc link voltage controller regulates the machine output dc link voltage via phase control and generates a firing angle reference (α) target for the machine. The current balancing algorithm generates firing angle trim components δ_i , for each set of the paralleled machine phases as depicted in figure 4.21. Thus, the compensated machine branch (i) rms current is now given by;

$$I_{ac_i} = \frac{I_{dc}}{2}\sqrt{\left[1 - \frac{\alpha - \delta_i}{\pi}\right]} \quad \text{for } i = 1 \text{ to } p \tag{4.31}$$

where, p is the number of parallel machine branch circuits, $p = 2$ for the topology depicted in figure 4.21. Bearing in mind that the machine dc link current for this current source topology may be actively controlled by the load converter, its imperative that the current reference signal for the current balancing strategy acts independently of the load current reference signal. Moreover, the reference current can be defined as an average load current $I_{ref}(t)$ of all the parallel branches as;

$$I_{ref}(t) = \frac{1}{p}\sum_{1}^{p} I_{fb}(t) \tag{4.32}$$

where, $I_{fb}(t)$ denotes the respective machine branch dc link current. Each machine branch has a dedicated controller that generates the current balancing trim component δ_i based on the error between the target current reference $I_{ref}(t)$ and its measured branch current feedback $I_{fb}(t)$. The trim component δ_i for each parallel branch is then subtracted from the global firing angle reference to generate the firing angle reference for all the phase H-bridge modules in that respective machine branch.

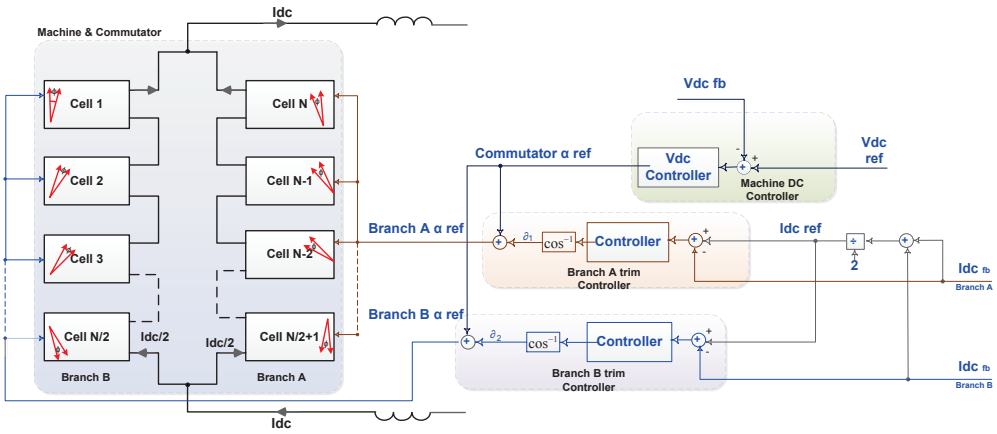

Fig. 4.21 Control Scheme for Balancing Machine Branch Currents

Figure 4.22 shows simulated waveforms when one phase voltage in machine branch B is permanently reduced to 90% of the normal phase voltage. Without any current balancing control, machine branch B will take a greater proportion of the dc link current. The waveforms show the impact of the current balancing control scheme when its enabled at $t = 1s$ and disabled at $t = 2.52s$ and re-enabled at $t = 3.5s$. It is clear from the waveforms that the current balancing scheme does not only successfully balance the machine branch currents but also damps the second harmonic ripple frequency component in the branch current that would otherwise exists due to the current imbalance.

Machine & Commutator Faults Detection

Typical faults on machine and converter can be broadly grouped into short circuit faults, open circuit faults and earth faults.

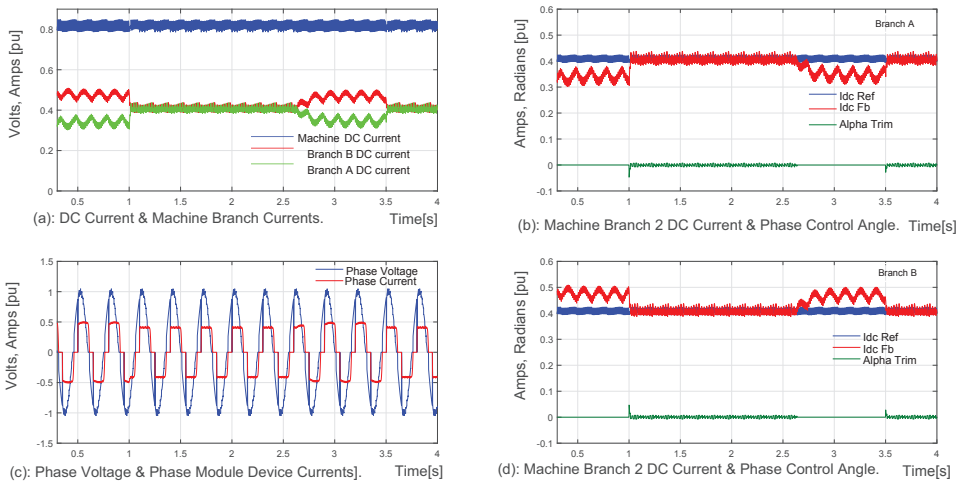

Fig. 4.22 24 Phase Multilevel topology; Simulated Machine Branch Current Balancing Control.

- **Earth faults** can cause additional insulation stresses on the machine and converter components. As such the machine and converter components can be selected to withstand the additional voltage stress due to earth faults to facilitate continuous operation under earth fault conditions. To a larger extent the voltage stresses are subject to the system earthing strategy employed. Since the proposed machine topologies do not feature any neutral star point, the system can be effectively earthed on the dc mid point thereby minimising the common mode voltage magnitude seen by the machine and its associated power electronics.

- **Short circuit faults** can cause over-currents and additional thermal stresses on the machine and associated converter. The most likely place for short circuit faults to occur is in the converter particularly if Thyristor type devices which fail to short circuit are employed. In this case line fuses can be employed to open circuit the failed module of the converter and turn the short circuit fault into an open circuit fault.

- **Open Circuit faults** Can occur in the converter for example when a device fails to turn on due to gating system failure. The proposed topologies can employ control schemes to enable continuous operation with one or more converter phase modules open circuited.

In this machine topology, most of the machine and H-bridge phase module faults, either open circuit, short circuit faults or other H-bridge mal-operational faults generally result in machine branch currents imbalance between the paralleled branches. Machine branch current parity detection can be conveniently applied to rapidly detect and shutdown the machine phase H-bridge modules or activate the fault tolerance machine operating mode. In this case the individual machine branch currents can be compared against the average machine current to ensure they are within the expected healthy thresholds. As such, from a machine protection view point, it is not necessary to measure the individual machine phase module currents and voltages. This significantly easies the cost and footprint of voltage and current sensors required, bearing in mind the large number of machine phases involved.

Machine Topology Fault Tolerant Operation

Fault tolerance capabilities of multilevel converter systems have been widely acknowledged and reported [130, 131, 102, 103, 132, 133]. The multiphase multilevel topologies presented here also benefit from the fault tolerance capability of multilevel systems. For fault tolerance to be achieved in the machine and converter topologies being considered here, machine phase H-bridges with load current freewheeling paths are mandatory as they are essential in allowing the load current to bypass the faulty phase circuits. Obviously topologies (b), (c) and (d) in figure 4.18 have inherent freewheeling path which facilitate fault tolerance as the phase modules can naturally bypass open circuit phase faults without the need for triggering H-bridge devices. To illustrate the fault tolerance ability of this topology, two cases have been analysed and simulated, one with a partial loss of a machine phase module and one with a complete loss of a phase module.

Operation With Machine Phase H-bridge Partial Loss. Partial loss of a machine phase H-bridge will result in an imbalance of the machine branch currents and can create an undesirable fundamental harmonic component in the machine branch output dc currents. The current balancing algorithm proposed in the preceding section can be effectively applied to enable continued machine operation with this machine phase fault. Figure 4.23 shows simulated response of the current balancing algorithm to a

single machine phase H-bridge open circuit fault where power electronic device of a phase H-bridge arm fails to turn on, eg due to a device gating fault. With the current balancing control enabled, a phase arm open circuit fault is applied at $t = 1.22s$. It can be seen that this strategy is effective at balancing the machine branch currents thereby avoiding an over-current condition and consequent thermal stresses or cascaded failure of machine branch switching devices. Infact, the machine continues to operate successfully, with a significant reduction of the fundamental harmonic ripple current component in the branch output dc current. In this simulated case of an H-bridge arm open circuit fault, the effect of operating without the current balancing strategy is clearly visible when current balancing control is inhibited between $t = 3.5s$ to $t = 4.7s$. It is clear that machine availability can be significantly improved due this fault tolerance capability of the multiphase multilevel topology and current balancing algorithm.

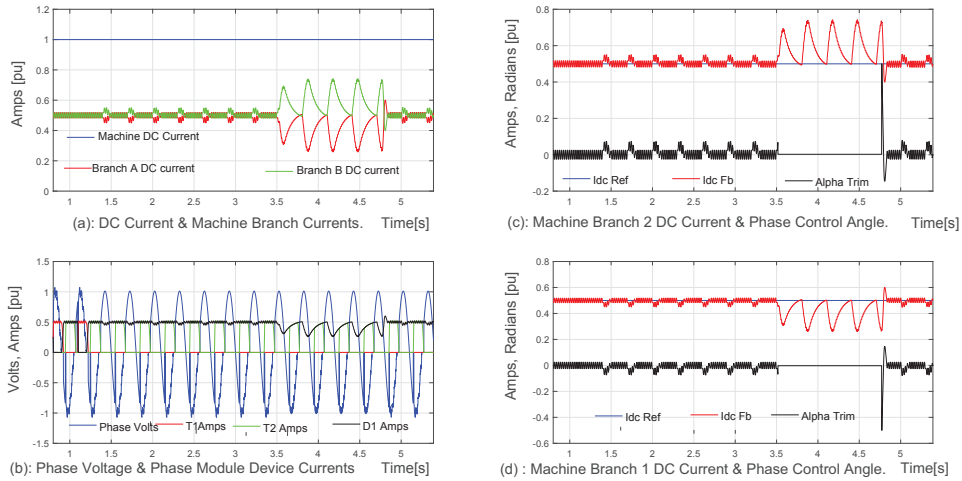

Fig. 4.23 Partial Loss of Machine Phase H-bridge due to Arm Device Failure

Operation With Machine Phase H-bridge Total Loss. Complete open circuit loss of a machine phase will also lead to branch current imbalance condition and will create a dominant second harmonic ripple component in the machine branch output dc currents. In this case the machine can still continue to operate owing to the available phase module's freewheeling path which can still bypass the faulty phase and continue to carry the load current, albeit with significant current imbalance between paralleled machine branch circuits. If not addressed, this can also lead to over current condition

and undesirable thermal stresses on the machine and power electronics components leading to reduced long term reliability of the drive system.

Figure 4.24 shows simulated waveforms when a machine phase winding open circuit fault is applied at $t = 1.4s$ with the current balancing technique enabled. The current balancing compensation is then disabled for the interval $3.5s \leq t \leq 4.6s$. The current balancing technique effectively applies corrective action to ensure balanced machine phase rms currents in addition to significantly reducing the second-harmonic dc link current component in the machine branch outputs. An additional benefit of the proposed current balancing compensation technique is the reduction in the magnitude of the machine electromagnetic torque ripple when operating with such machine faults, similar to that reported in [132].

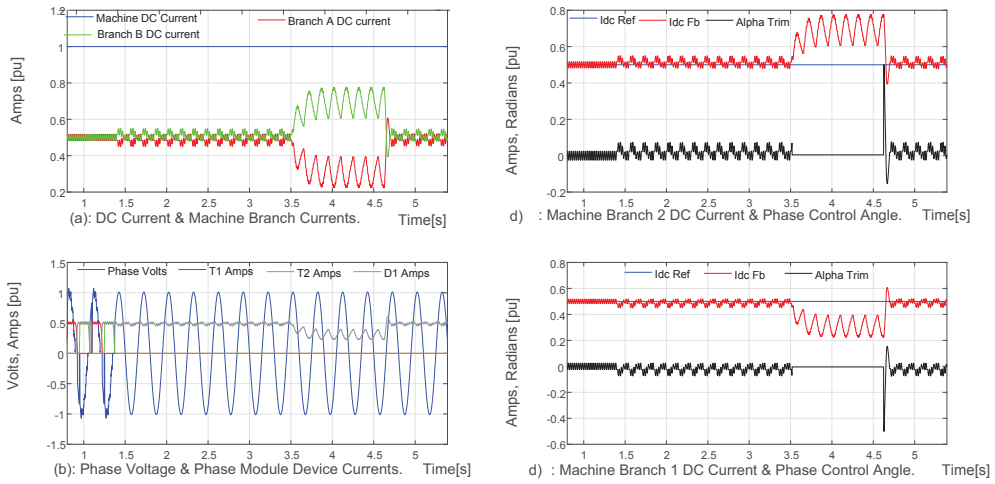

Fig. 4.24 Complete Loss of Machine Phase H-bridge

4.5.2 H-Bridge Vdc/Idc Two Quadrant Active Commutator

The analysis so far has only considered single quadrant operation, i.e. generating mode of operation for this multilevel multiphase machine topology. In this section, the analysis will be extended to full four quadrant operation, i.e. both generating and motoring applications such as propulsion drive systems and some renewable generating systems with some requirements for limited motoring mode to allow generator maintenance. Its worth bearing in mind that for this current source topology, the four quadrant torque/speed range is confined to two Vdc/Idc quadrants of unidirectional output dc

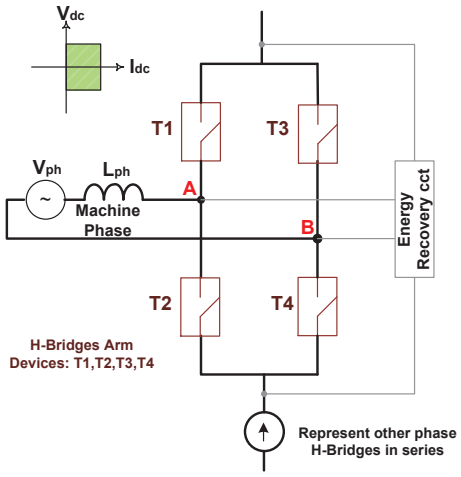

Fig. 4.25 Single Machine Phase & H-bridge Converter Cell

current and bidirectional output dc link voltage. As such machine phase H-bridge devices with reverse voltage blocking capability will be applicable. In this topology, all machine phase H-bridge arm devices are gate triggered. In cases where the machine commutating inductance is small, i.e. where its impact on output voltage regulation is negligible, semiconductor devices capable of natural commutation only such as Thyristors can be employed. However, if the machine commutating inductance is not negligible, semiconductor switching devices with forced current turn of capability will be required.

Natural commutation topologies will not be addressed further as their operational features are similar to those already presented in the preceding sections. Instead, forced commutation H-bridge topologies will be examined. Figure 4.25 shows a single phase H-bridge with gate triggered phase arm devices T1, T2, T3 & T4. In this case its assumed that semiconductor switching devices with gate triggered forced current turn off and reverse voltage blocking capabilities such as Gate Turn Off Thyristors (GTO), Integrated Gate Commutated Thyristors (IGCT), Reverse Blocking Insulated Gate Bipolar Transistors (RBIGBT), Metal Oxide Field Effect Transistors (MOSFET) with series blocking diodes, etc will be applicable. The H-bridge devices are phase controlled to either operate in inverting or rectifying mode i.e. motoring or generating mode respectively.

Single H-bridge Cell Operation

Carrying out Fourier analysis similar to that conducted for the half controlled topology shows that the peak amplitude of the individual voltage harmonic (k) relative to the maximum dc link voltage variation with firing angle α is given by;

$$V_k = \frac{\sqrt{2}}{k^2-1}[k^2\sin(\alpha)^2 + \cos(\alpha)^2]^{\frac{1}{2}} \tag{4.33}$$

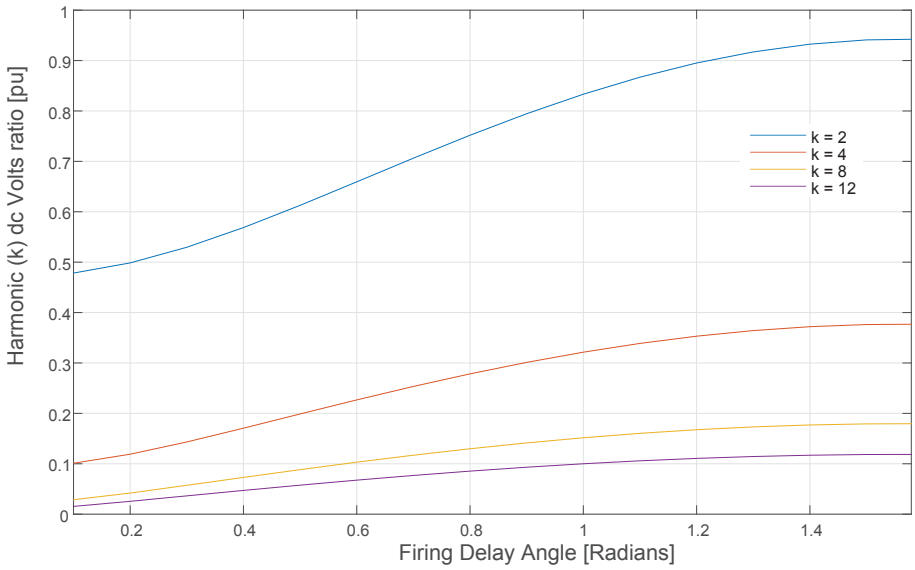

Fig. 4.26 Variation of H-bridge Output DC Individual Harmonic (k) with Firing Angle

Figure 4.26 shows the graphical representation of (4.33) for firing angle α variation between zero and $\pi/2$ radians. Comparison of the half controlled single quadrant topology harmonic characteristics of figure 4.19 with those this full controlled two quadrant figure 4.26 shows that the half controlled topology produces significantly less ripple than this full controlled equivalent. The harmonic performance superiority of the half bridge topology can be attributed to the freewheeling diodes in the half controlled bridges which provide alternative load current paths during certain intervals of the fundamental cycle. As already alluded to in earlier discussions, inclusion of flywheel diode across the d.c. terminals of a fully controlled bridge implies restricted operating mode to single quadrant as negative voltage cannot be developed.

Close analysis of the operation characteristics of the two quadrant H-bridge topology operation shows that it is possible to obtain improved harmonic performance in

this two quadrant topology by modifying the gating control sequence of the H-bridge devices to mimic the behaviour of the half controlled topology. Similar to the strategy presented in [134], for positive output voltages the use of modified H-bridge gating control sequence not only obviates the need for a freewheeling diode inherent in the half bridge topologies but also allows the same effect to be achieved in the negative output voltage quadrant. This may be achieved by recognising that any of the pairs of series H-bridge arms of a fully controlled bridge may be triggered together at the zero-voltage instants such that the series H-bridge arms act as a single free-wheeling diode.

With reference to figure 4.25, the operational state of the H-bridge can be grouped into active voltage vector states and passive voltage vector states. Active voltage vectors are obtained when either device pairs (T1,T4) or (T2,T3) are turned on, i.e. when the machine phase is connected to the output load. Zero vector states are obtained when phase H-bridge series arm devices (T1,T2) or (T3,T4) are turned on, i.e. the machine phase is bypassed by a freewheeling path. Assuming a sinusoidal voltage across machine phase terminals A and B of the machine H-bridge cell depicted in figure 4.25, the voltage across the H-bridge cell ac terminals V_{AB} given by;

$$V_{AB} = V_{ac}\sin(\theta) \tag{4.34}$$

where, V_{ac} is the peak voltage. This can be represented as the difference of two voltages V_A and V_B with half the amplitude of V_{AB} and phase displaces by π radians as;

$$V_A = \frac{V_{ac}}{2}\sin(\theta_A) \tag{4.35}$$

$$V_B = \frac{V_{ac}}{2}\sin(\theta_B) \tag{4.36}$$

where, $\theta_A = \theta + \varphi$, $\theta_B = \theta + \pi + \varphi$ and φ is the phase displacement of the respective machine phase winding connected to the H-bridge and θ is the fundamental machine voltage angle. If the effect of commutating inductance is neglected, two phase control angles β and γ can be defined such that the H-bridge output dc link voltage is expressed as;

$$V_{dc} = \frac{V_{ac}}{\pi}[\cos(\gamma) - \cos(\beta)] \tag{4.37}$$

where, β controls when the H-bridge active vectors (T1,T4) and (T2,T3) are activated and γ controls when the zero vectors (T1,T2) or (T3,T4) are activated relative to the fundamental angle θ.

Positive DC Output Voltage. Its clear from examination of (4.37) that if $\gamma = 0$, the H-bridge output dc link voltage can be controlled from zero to maximum positive value by varying the phase angle β from zero to π. Figure 4.27 shows the H-bridge device switching pattern for the active and zero vectors over the fundamental period for positive output dc link voltage. In this case, the point at which the zero vector states are activated is fixed at $\theta_A = 0$ and $\theta_B = 0$. The positive dc link voltage is controlled by varying the point at which the active vector states are activated, i.e. by varying the control angle β. This switching pattern gives the same desirable power factor and output voltage harmonics operational characteristics as the half controlled bridge discussed earlier.

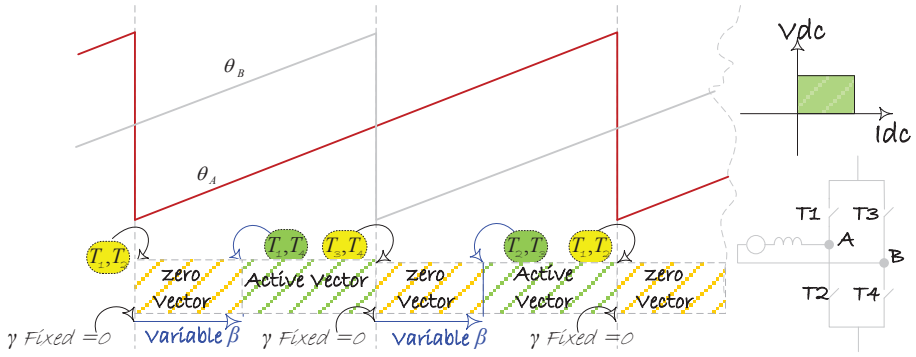

Fig. 4.27 H-bridge Control Sequence for Positive Output DC voltage

Negative DC Output Voltage. Similarly, if $\beta = 0$, the H-bridge output dc link voltage can be controlled from zero to maximum negative value by varying the phase angle γ from zero to π. In other words β controls the point at which the active vector states are inserted and γ controls the point at which the zero vector states are inserted

relative to the fundamental voltage phase angle. Figure 4.28 shows the H-bridge device switching pattern for the active and zero vectors over the fundamental period for negative output dc link voltage. In this case, the point at which the active vector states are activated is fixed at $\theta_B = 0$ and $\theta_A = 0$. The negative dc link voltage is controlled by varying the point at which the zero vector states are activated, i.e. by varying the control angle γ. The choice of which active states to apply is chosen based on whether positive or negative output dc link voltage is required.

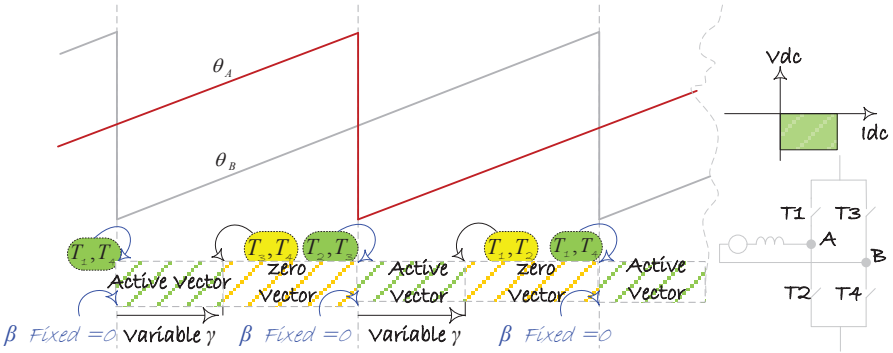

Fig. 4.28 H-bridge Control Sequence for Positive Output DC voltage

With this control strategy, the desirable characteristics of the half controlled H-bridge regarding improved dc voltage ripple harmonics and better power factor are obtained without restricting the operating modes to a single quadrant generating mode. Additionally, this strategy minimises the H-bridge device switching losses due to only one H-bridge arm device switching per given switching vector transition. Owing to the phase displacement between the machine phases, this control strategy leads to significant reduction in output voltage ripple harmonics when it is applied to multiphase machines. It also facilitates good machine operating power factor especially under conditions of high dc link current and low output dc link voltages, thanks to the zero voltage vector states.

4.6 Forced Commutation and Energy Recovery

The discussion so far has assumed the H-bridge cells power electronic devices operating under natural commutation. In cases where the machine commutating inductance is not negligible, operating in natural commutation mode can result in poor voltage regulation and reduced machine efficiency. To improve the machine operating performance, it may be necessary to employ forced commutation of the machine H-bridge semiconductor switching devices. This section considers the machine converter topologies capable of operation under forced commutation mode. Forced commutation brings with it some challenges that will need to be overcome for successful machine operation. The main challenge is to do with how the energy trapped in the machine commutating inductance is managed during the forced commutation intervals. This section will briefly explain the proposed machine H-bridge cells commutation process and discuss potential energy recovery circuits that can be employed to maximise machine efficiency.

4.6.1 Single H-bridge Cell Commutation Process

A summary of the operation and forced current commutation process of a phase H-bridge cell is given in this section. It is assumed that the machine phase commutating inductance is not negligible, i.e. for desirable operational performance of the machine, there is a need for forced commutation of the phase current. It is also assumed that dc current in all the other H-bridges connected in series with the H-bridge undergoing commutation will stay constant during the commutation process. At this stage, attention is given to the forced commutation operation only, the energy recovery circuit operation is ignored for now. For this multilevel multiphase machine converter topology, all machine H-bridge cells operational characteristics are exactly identical. As such, a single machine phase and its associated H-bridge cell will be considered.

Although a generating mode topology is used here for illustration purposes only, similar operational characteristics will apply for the motoring mode. Figure 4.29 below shows the power electronic circuit topology of a single machine phase winding and its H-bridge converter cell. The machine phase voltage and machine commutating inductance is represented by *Vph* and *Lc* respectively. The power devices T1, T2, T3

& T4 although assumed to be of a Thyristor type with forced commutation capability, any semiconductor power electronic device with reverse voltage blocking and forced commutation capability can be used. These devices are configured to form the machine phase power electronics H-bridge cell. In this generating topology, an extra diode *D1* has been included to reduce conduction losses during the zero vector states.

The diode rectifier comprising of *d1,d2,d3,d4* and its output capacitor *C-clamp* forms the voltage clamping circuit for the H bridge cell which is essential for absorbing the energy ($(0.5L_c i^2)$) trapped in the machine phase commutating inductance during the commutation process. The energy transferred to the clamp circuit can then be either recovered by the energy recovery circuit or wastefully dissipated resistively as heat. The commutation process described in the subsequent sections will reference the circuit component labelling highlighted in figure 4.29.

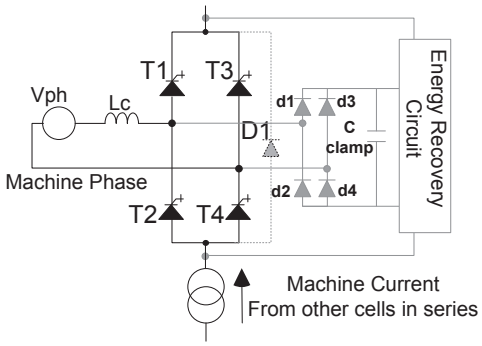

Fig. 4.29 Machine H-bridge cell with Voltage Clamp and Energy recovery Auxiliary circuits

When the current commutation occurs, the machine phase current polarity reverses. The rate at which the phase current commutates depends on the voltage available to aid commutation, the magnitude of the phase current and the effective commutating inductance of the respective machine phase undergoing commutation. The machine phase winding current reversal commutation process is illustrated in a number of H-bridge device states below.

Commutation Sequences Reference to figure 4.30 will be made in the explanation of the commutation stages. It is assumed that before the start of the commutation

process, the H-bridge devices T2 & T3 are ON and carrying the machine phase winding current and at the end of the commutation process devices T1 & T4 will be ON and carrying the machine phase winding current in the opposite direction.

State 1: Commutation starts with T2 & T3 ON and carrying phase current. Subject to the operating firing angle, the current may start naturally commutating into diode D1 at this stage if the voltage is sufficient to forward bias the diode.

State 2: Starts when device T1 is fired resulting in three devices being ON (T1, T2 & T3). When T1 is fired, current does not immediately transfer from T3 to T1 instantly. In fact the current will stay in T3 until the phase voltage reaches a sufficient level for diode D1 to become forward biased and the current will then starts to naturally commutate from T3 to D1. An interval when either both the top or bottom arms of the H-bridge cells are ON at the same time will be referred to as the overlap period. In this case both T1 & T3 devices are ON.

State 3: At this stage, the phase current still has not reversed polarity and device T3 is now force commutated. At this point, separate current paths are formed: most of the constant load current from other seriesed H bridge cells not undergoing commutation diverts into the diode D1 and a small fraction (if any) diverts into T1 (dictated by magnitude of on state voltage drop of 2 series devices T1 & T2 versus one diode D1). The clamping circuit diodes d2 & d3 become forward biased and all the phase winding current of this cell undergoing commutation is rapidly diverted into the clamp circuit and charges up the clamp capacitor, C-clamp. In this state, the energy trapped in the machine inductance is transferred to the cell clamp capacitor and increases the capacitor voltage up. At this stage, the rate of change of the phase winding current is strongly influenced by the voltage difference between the peak phase voltage and the clamp capacitor voltage magnitude. The phase winding current continues to be diverted into the clamp circuit and will eventually get to zero and stays at zero, assuming no other devices are switched. This state creates a zero vector state where the load current bypasses the respective machine phase winding, i.e. machine phase is essentially open circuited and no phase current is present. The duration of this

zero vector state can be beneficially exploited to aid regulation of the machine average output power.

State 4: At this stage, device T4 is now fired. Again the period when both T2 & T4 are ON is another overlap time state. When T4 is turned on, current will now start to naturally commutate from diode D1 to the H-bridge phase, subject to magnitude of phase voltage.

State 5: T2 is turned OFF at this stage. Note, since most of the current from other seriesed H-bridges will be through D1, the devices T4, T2 will have very low or no current at this stage, so T2's forced commutation duty is very low, i.e. force commutates very low current if any.

State 6: The current in D1 has effectively naturally commutated to zero and devices T1 & T4 now carry the phase current. This completes the H-bridge cell current commutation process.

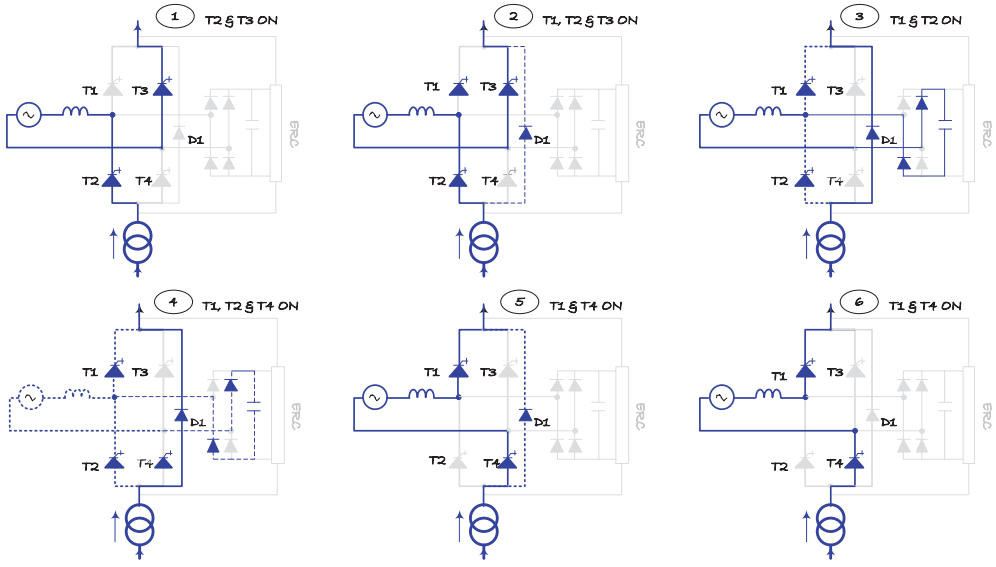

Fig. 4.30 Phase Cell H-Bridge Cell Commutation Sequence States

Device Commutation Duty It can be noted that in the example illustrated in figure 4.30 , the commutation started with T2 & T3 ON, of these two devices the device that turns off first (T3 in this case) always force commutates a significant amount of current

State	**State 1** (active vector)	**State 2** (overlap)	**State 3** (zero vector)	**State 4** (overlap)	**State 5 & 6** (active vector)
Sequence 1	T_2, T_3	T_1, T_2, T_3	T_1, T_2	T_1, T_2, T_4	T_1, T_4
Forced Commutation		T_3		T_2	
Sequence 2	T_2, T_3	T_2, T_3, T_4	T_3, T_4	T_1, T_3, T_4	T_1, T_4
Forced Commutation		T_2		T_3	

Table 4.1 Alternative Forced Commutation Sequences and Active & Zero Vector States

in comparison to the other device (T2 in this case). This commutation characteristic has a direct impact on the duty and rating of the device gating system if Thyristor type devices with gate assisted current commutation are used. For such cases, in order to ensure that all devices and their associated gating systems are equally exercised during the operation of the machine, the commutation phase sequence can be made to alternate between sequences 1 & 2 highlighted in Table 4.1 below.

A similar alternating commutation sequence can also be deduced when the current polarity is opposite, i.e. start commutation with devices T1 and T4 ON. Thus, for a given phase current over two fundamental cycles all four arms of the H-bridge cell will have undergone the same forced commutation duty.

Analysis of the operational characteristics shows that apart from the machine commutating impedance, phase voltage and load current, there are three other parameters that also affect the behaviour and performance of the machine, namely; the operating phase control angle (α), the commutation overlap period and the commutation zero vector state periods. These parameters add extra degrees of freedom that can be exploited to give desired optimum machine and converter operating performance.

It can be readily appreciated that instead of employing the above commutation sequences and strategy, where all four arms have the same forced commutation duty, alternative commutation strategies where either only the top or bottom arms of the H-bridge cell are force commutated is also feasible. For applications requiring single quadrant mode of operation, the other arms can be naturally commutated and employ simple diodes or Thyristors with no controlled current turn off capability as highlighted in earlier sections. This can be beneficial in applications where simplicity and reliability of the H-bridge cell is of paramount importance. In this case current control is achieved by the two arms of the H bridge cell with controlled gate turn on/off functionality.

However, as alluded to earlier, this simplicity comes at the expense of the possibility of inability of the converter cell to interrupt fault current under certain converter cell failure modes, such as short circuit device failure on the arms with current turn off capability.

4.6.2 Proposed Energy Recovery Circuit Topologies

To increase the overall machine and converter efficiency during phase current commutation events of the machine phase converter H-bridge cells, instead of wasteful resistive dissipation of energy transferred into the clamp circuits during commutation periods, energy recovery circuits can be employed to recover the energy back into the drive circuit. The need to increase efficiency by recovering the commutation energy has been acknowledged in past research work [135–138]. However, most of this work has focused on one drive topology, namely the three phase Line Commutated Inverter (LCI) drive topology. Although the energy recovery topologies reported in this earlier work do not lend themselves for direct application to the multilevel multiphase topologies considered in this work, the concepts can still be modified and adopted to achieve similar energy recovery function.

Since the energy transferred into the clamp circuit varies proportionally with the commutating inductance and the square of phase current being commutated, actively controlled energy recovery circuits will be required to enable clamp voltage control. A number of energy recovery topologies have been considered in this work. A few of these will be examined in the following sections.

Forward Converter Energy Recovery Circuit

A switch mode power supply type energy recovery circuit can be adopted to recover the energy transferred to the clamping capacitor from the machine phase leakage inductance during phase current commutation. Two types of switch mode converters, forward converter and flyback converter are typical candidates for this energy recovery circuit. The Key desirable attributes of the chosen circuit are:

(a) The galvanic isolation between the clamping circuit and the energy recovery interface circuitry.

(b) The simplicity of the circuitry with a few actively controlled switching devices.

(c) The ability to produce controlled output voltage.

A forward converter switch mode power supply topology has been considered for the energy recovery circuit. The forward converter topology is generally more efficient in comparison to flyback converter topology for the anticipated energy recovery duty. Additionally, forward converter transformers have less leakage inductance, thus require smaller snubber circuits in comparison to the flyback converters due to the lack of large air-gap in the mutual flux path.

To simplify the forward converter energy recovery circuit analysis, it can be assumed that the forward converter transformer has no net magnetising ampere-turns, no energy is stored in the transformer core, no leakage fluxes exist and the transformer has zero magnetising current. In the practical implementation of this circuit however, some leakage reactance and magnetising current will be present; as such these secondary attributes will be examined in the detailed analysis of the circuit at a later stage once the initial viability of the concept is established. In the interest of clarity, a forward converter topology with a single active switch has been used to access the topology viability; other forward converter topologies are equally applicable.

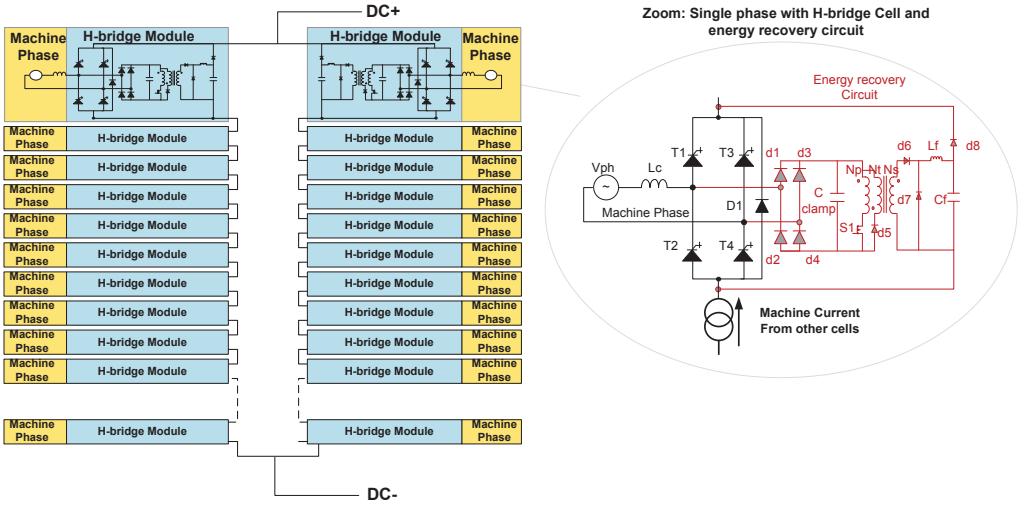

Fig. 4.31 Multiphase multilevel Topology with Forward Converter Energy Recovery Circuit

A forward converter energy recovery circuit highlighted in Figure 4.31 is examined in more detail to fully characterise its operation. The circuit comprises of a forward converter transformer with a primary winding (N_p), a secondary winding (N_s) and a tertiary winding (N_t). It is assumed that the primary and tertiary windings are tightly coupled, i.e. bifilar winding. The primary winding is in series with an actively controlled PWM switch (S_1) and the tertiary winding in series with a freewheeling diode (d_5) meant to provide a path for recovering the magnetisation and leakage energy, i.e. transformer magnetisation reset. The maximum achievable PWM duty cycle (δ) is given by $\delta = Np/(Np+Nt)$ and this relationship constrains the maximum achievable duty cycle. Higher tertiary winding turns implies low switch S1 voltage stress and low duty cycle and power output but increases the voltage stress on the diode (d_5).

In this analysis, it's assumed that the primary and tertiary windings have the same number of turns, which implies a 50% theoretical maximum achievable duty cycle. A high switching frequency of circa 20 kHz is envisaged for such a topology to reduce the size of the magnetic wound components. Lower switching frequencies are undesirable as they can result in higher peak forward converter currents and can potentially cause the clamp capacitor to discharge to voltage levels far below the peak of the machine phase voltage thereby negatively impacting the overall efficiency of the system as will be shown later. The diodes (d_6) & (d_7) together with the output filter (L_f) & (C_f) and a diode (d_8) form part of the interface circuit for recovering the energy back into the machine circuit.

To minimise losses with the proposed energy recovery circuit, the clamp capacitor voltage must always be kept greater than the peak of the phase voltage, otherwise clamp diodes will become forward biased and the clamp circuit will start accepting power from the respective machine phase during non-commutation intervals. In essence, the clamp circuit is only intended to absorb energy during the commutation events in order to clamp any over-voltages that may occur across H-bridge cell switching devices during forced commutation events. Therefore, clamp capacitor voltage regulation by the forward converter is imperative in this topology.

The operating principle of the stand alone forward converter is well documented in literature [139–144] and will not be repeated here. Only its functional adaptation for the energy recovery circuit in this machine/converter topology will be explored. The energy

recovery action is only activated once the commutation process is complete, as such, the forward converter PWM pulses to switch (S_1) are inhibited during commutation events. Having alluded to the need for regulating the clamp capacitor voltage, the switch (S_1) is PWM controlled to regulate the clamp voltage such that:

(a) Its magnitude is always above the peak of the phase voltage. A reference voltage above the peak phase voltage is required. This can be guaranteed by using a sufficiently high constant threshold or by programming the voltage threshold as a function of the machine speed for a given machine operating flux level.

(b) It discharges the clamp capacitor to the reference voltage level before the start of the next commutation event, else the clamp capacitor voltage will gradually pump up to levels beyond the safe operating area capability of the semiconductor switching devices of the machine H-bridges. The clamp voltage controller can either be a conventional proportional plus integral type or a hysteresis bang-bang type controller.

Forward Converter Energy Recovery States

This section gives a summary of the energy recovery circuit states. It's assumed the commutation process for the respective H-bridge cell is complete and the clamp capacitor has been charged up to a much higher voltage than the peak phase voltage. The operational states are depicted in figure 4.32, bearing in mind the energy recovery action is only activated when the phase current is not undergoing commutation, i.e. no H-bridge device switching event occurs during energy recovery.

State 1: The energy recovery event starts when the PWM switch S_1 is turned ON and the clamp capacitor current flows through the transformer primary winding thereby transferring energy to the tightly coupled secondary winding into capacitor C_f through diode D_6, and smoothing inductor L_f.

State 2: PWM switch S_1 is turned OFF; the energy trapped in the leakage and magnetising reactances of the forward transformer is freewheeled via the tertiary winding and diode D_5 into the clamp capacitor. Diode D_7 provides a freewheeling path for the current trapped in the output filter inductor L_f.

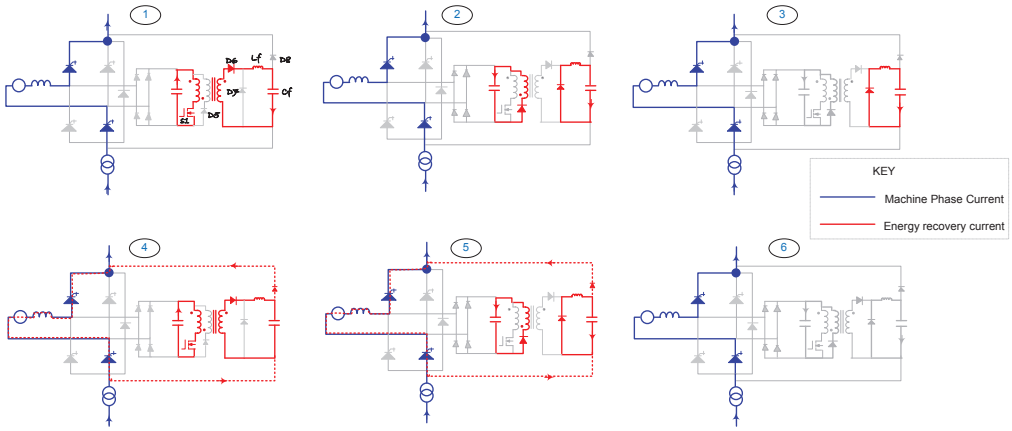

Fig. 4.32 Forward Converter Energy Recovery Circuit Operation States

State 3: The current in the tertiary winding rapidly decays to zero. The output filter inductor current continues to decay via D_7, L_f and charges the capacitor C_f.

State 4, 5: States 1 to 3 are repeated several times at PWM switching frequency until the forward converter output filter capacitor C_f voltage exceed the peak of the phase voltage. At this stage the filter capacitor C_f starts discharging through the H-bridge into the machine phase winding. The forward converter will eventually be inhibited when the clamp capacitor dc link voltage gets to the target voltage threshold which should be above the peak of the machine phase voltage.

State 6: At this stage the clamp capacitor voltage has discharged to its voltage reference threshold and the energy recovery circuit is turned off.

Figure 4.33 shows the simulated waveforms of a machine phase H-bridge including the phase current commutation events and the energy recovery periods. The top plot shows the machine phase voltage and clamp circuit capacitor voltage, the bottom plot shows the machine phase current and clamp capacitor current. It can be seen that during phase current commutation, the clamp capacitor voltage rapidly increases due to energy transfer from the machine commutating inductance into the clamp capacitor. The machine phase terminal voltage is clamped to this peak value, seen by spikes on the voltage waveforms during commutation events. The period between commutation events is when the forward converter is transferring the energy from the clamp capacitor to the output of the forward converter. Figure 4.34 shows a zoomed

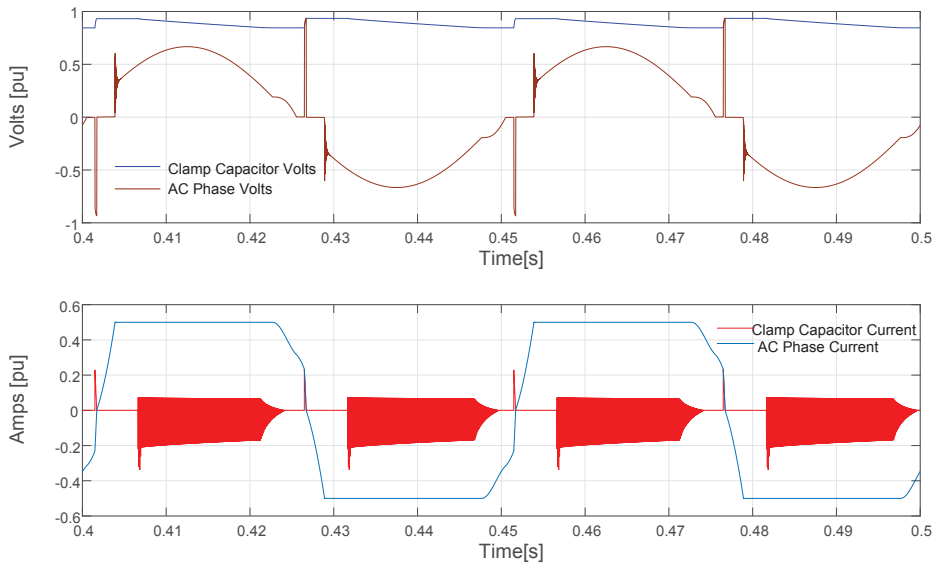

Fig. 4.33 Forward Converter ERC Clamp Capacitor Volts, AC Phase volts & Clamp Capacitor Amps

version of figure 4.33 when the forward converter is active, seen by the negative pulse width modulated clamp capacitor current.

Figure 4.35 shows the corresponding machine H-bridge currents, forward converter currents and the machine phase voltage and current for the same period as figure 4.33. The top two plots(a) and (b) show the H-bridge device currents. The third plot (c) shows the currents in the forward converter switching device S_1, freewheeling diode $D5$ and in the diode $D8$ which conducts the recovery energy back into the drive circuitry. As can be seen in plots (c) and (d), the recovered energy is pumped back into the drive circuit when the voltage of the forward converter output capacitor C_f exceeds the peak of the machine phase voltage and forward biases the diode $D8$. This has the effect of increasing the voltage across the machine phase and initiate current commutation. Figure 4.36 shows a zoomed version of figure 4.35 when the forward converter is active, seen by the pulse width modulated current of the forward converter switch S_1 and freewheeling diode D_5.

The forward converter presented above is very effective at recovering the commutation energy but suffer the drawback of being limited to one quadrant generating operating mode only. Owing to the polarity reversal of the dc link voltage required for inversion mode of operation, this energy recovery topology would not be applicable.

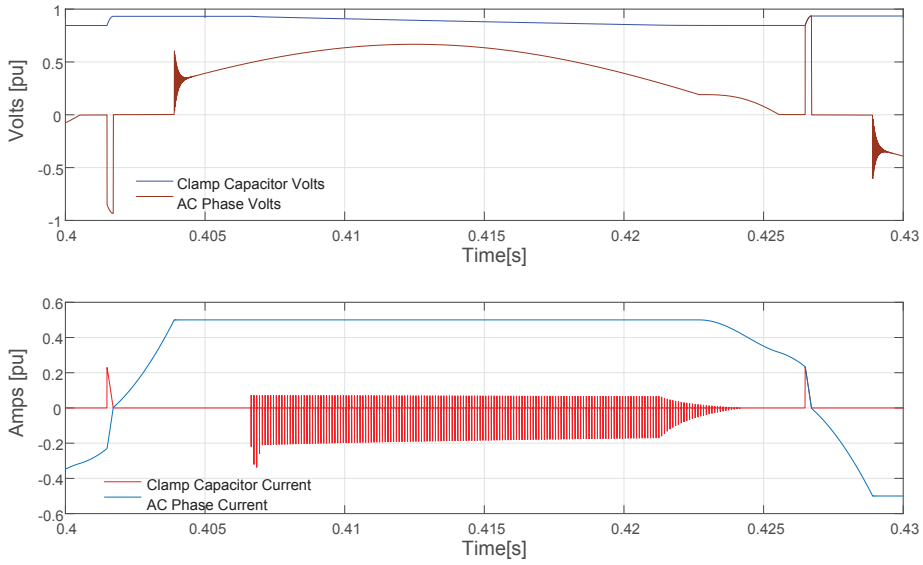

Fig. 4.34 Forward Converter ERC Clamp Capacitor Volts, AC Phase volts & Clamp Capacitor Amps

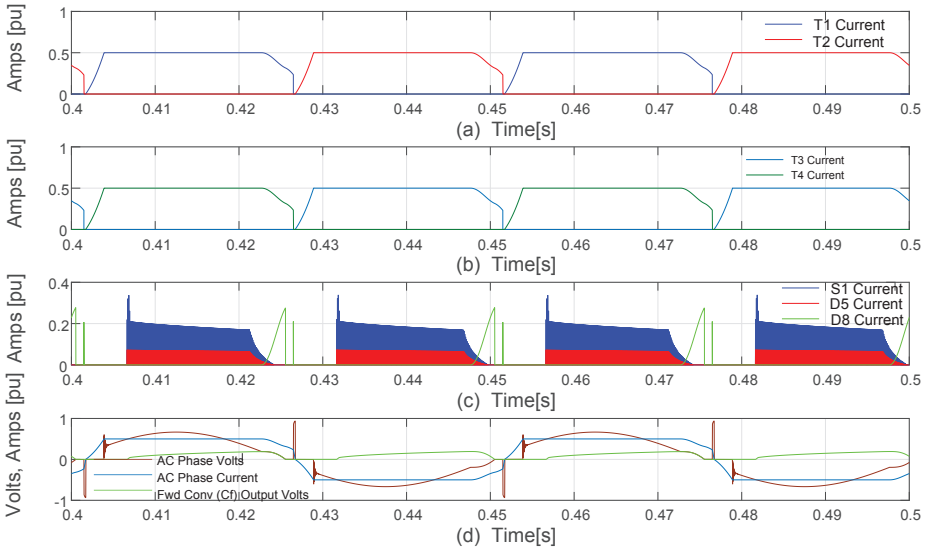

Fig. 4.35 Forward Converter ERC Clamp Capacitor Volts, AC Phase volts & Clamp Capacitor Amps

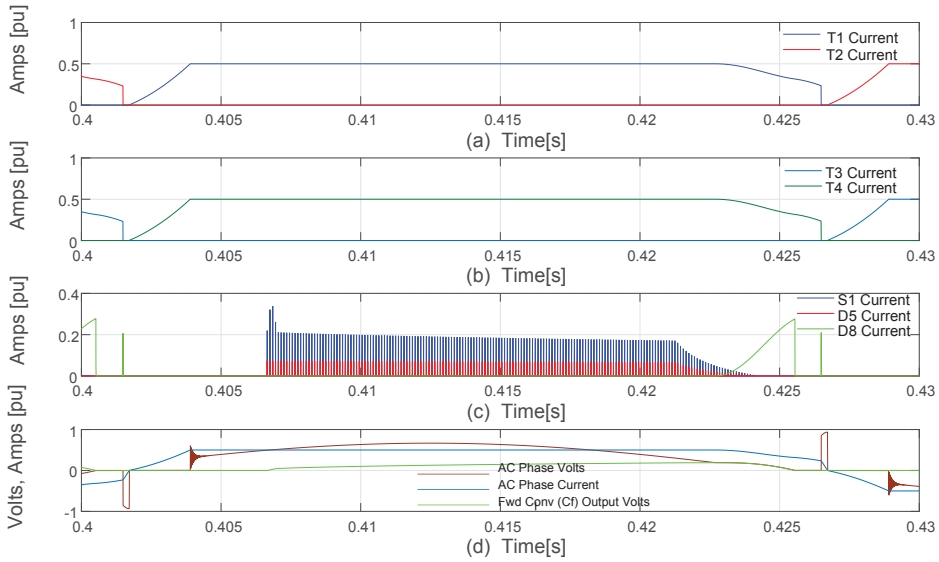

Fig. 4.36 Forward Converter ERC Clamp Capacitor Volts, AC Phase volts & Clamp Capacitor Amps

In some cases, subject to the amount of energy to be recovered, the forward converter can result in increased overall footprint of the energy recovery circuit owing to the use of wound components, i.e. its transformer and smoothing inductor, which can be bulky in some cases. An alternative attractive topology which does not employ wound components and does not suffer the restriction of one quadrant mode operation but is applicable to both the generating and inverting quadrants will now be examined next.

Voltage Source H-bridge Energy Recovery Circuit

The energy recovery and commutation circuits proposed for the LCIs presented in [135, 137, 138] have been realized based on complex circuit topologies which require a number of energy storage components, capacitive and inductive wound components. These are less attractive as they tend to adversely affect the reliability, cost and footprint of the overall solution. The proposal presented in [136] in which a three phase voltage source converter is employed to assist LCI converter Thyristor devices commutation when the machine back emf is low and also assist with energy recovery is more attractive owing to its simplicity and absence of wound components.

A similar topology, modified for the multilevel multiphase topology has been adopted for the energy recovery action in this work. A voltage source H-bridge

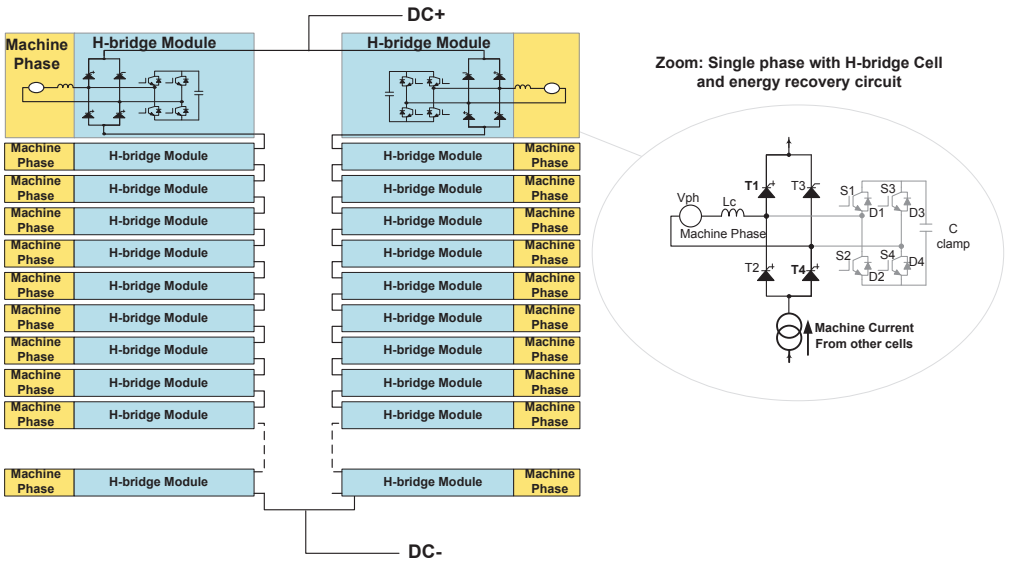

Fig. 4.37 H-bridge Energy Recovery Circuit Configuration.

converter energy recovery circuit highlighted in Figure 4.37 is examined in more detail to fully characterise its operation. This comprises of the diode rectifier and capacitor clamp circuit arrangement already presented in the forced commutation circuit description earlier. In addition, additional four switching devices are connected, one across each of the clamping diodes as shown in figure 4.38. Unlike the forward converter circuit discussed above, this proposed H-bridge energy recovery circuit topology only operates during short commutation instants of the machine phase current and handles a small portion of the load power. As such, switching components with low power rating are necessary for this energy recovery circuit.

The operation of the H-bridge ERC circuit is described with the help of figure 4.38. This circuit performs two distinct actions; (a) absorbing the energy trapped in the machine commutating inductance to snubber the potential destructive overvoltage that may result from forced current commutation, and (b) recovering that energy back into the drive circuit at appropriate intervals during the phase current reversal period. These two modes are:

Energy Recovery Mode: In this mode, the energy recovered back into the load circuit from the clamp capacitor C_{clamp} is the energy absorbed from the previous commutation interval of the machine phase H-bridge. This is represented by

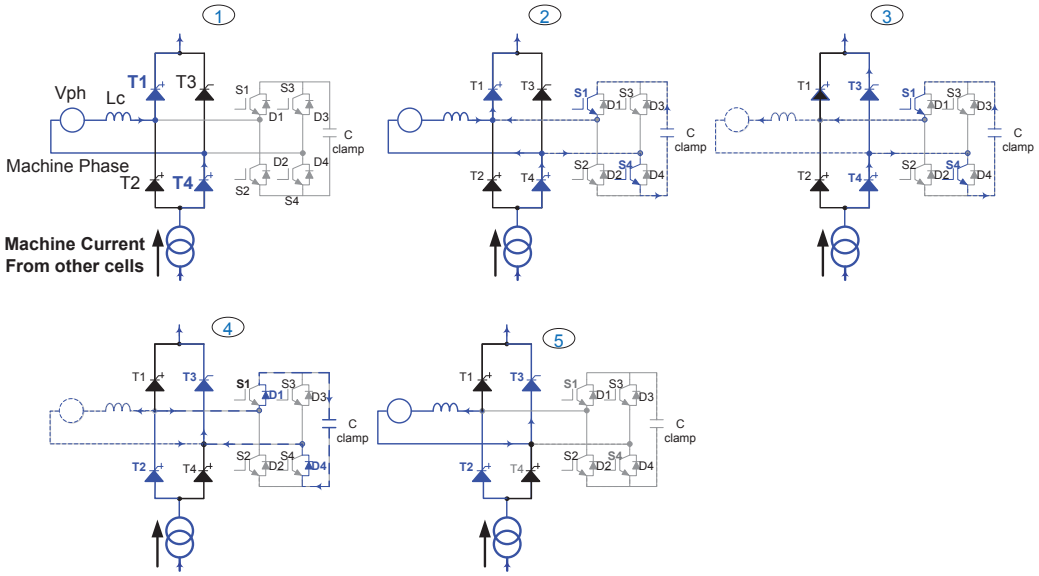

Fig. 4.38 H-bridge Energy Recovery Circuit Operation States.

states 2 and 3 in figure 4.38. When the energy recovery circuit devices S_1 and S_4 are turned ON, a proportion of the load current is diverted into the clamp circuit causing a negative current pulse to flow and discharge the stored energy in the clamp capacitor.

Figure 4.39 shows the simulated waveforms of the commutation and energy recovery events over a fundamental cycle. The top plot shows the clamp circuit capacitor voltage and machine phase terminal voltage. The bottom plot shows the machine phase current and the clamp capacitor current. As can be seen in these waveforms, the energy stored in the clamp capacitor is recovered into the load circuit, depicted by the negative pulse of load current in the clamp capacitor and a corresponding drop in the clamp capacitor voltage. The amount of recovered energy, hence, depth of clamp capacitor voltage discharge is controlled by the ON time duration of the energy recovery circuit devices. As highlighted earlier, the clamp capacitor should not discharge to a value below the peak of the phase voltage.

Figure 4.40 shows the phase H-bridge device currents, the energy recovery circuit currents and the machine phase voltage and current. It can be seen in this figure that the load current is diverted into the energy recovery circuit before

forced commutation of the main phase H-bridge devices. The energy recovery phase ends when the H-bridge device T_3 is turned ON to create a zero voltage state where, the load current is now freewheeled through H-bridge devices T_3 and T_4 as can be clearly seen in figure 4.41 which shows a zoom of the commutation interval depicted in figure 4.38.

Energy Absorption Mode or Voltage Clamping Mode: This stage occurs when the zero state vector interval is terminated, for example in stage 4 of figure 4.38. In this mode, the gate controlled energy recovery circuit devices are turned OFF, the current is conducted through the passive clamping devices, diodes D_1, D_2, D_3, D_4. This stage corresponds to the stage when the machine phase current is close to zero when device T_2 is turned ON and device T_4 is turned OFF, as can be seen in figure 4.40 and figure 4.41. The forced commutation of device T_4 causes rapid transfer of the load current into the clamp circuit. During this period, the load current which has diverted into the clamp circuit begins to transfer into the machine phase winding and ends when the entire rated load current is passing through the phase winding. The rate of rise of the phase current is dictated by the machine's commutating inductance and the clamp capacitor voltage level.

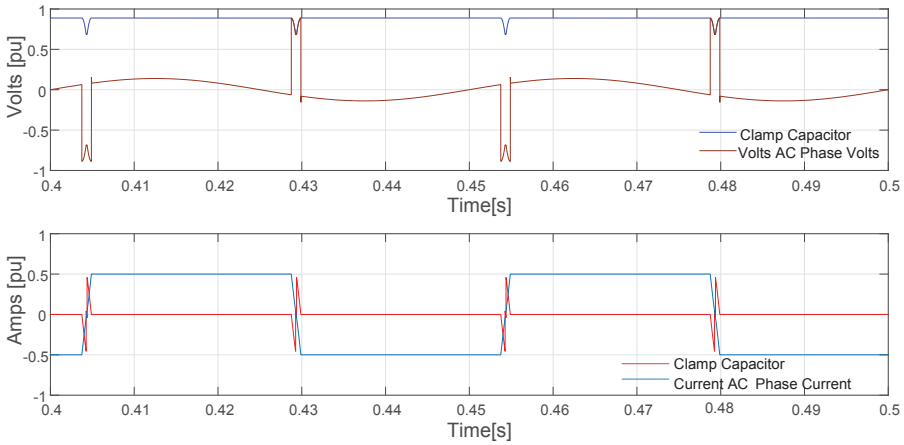

Fig. 4.39 H-bridge Energy Recovery Circuit: Clamp Capacitor Volts, AC Phase volts & Clamp Capacitor Amps.

The proposed voltage source H-bridge clamping and energy recovery circuit is effective at both clamping and recovering commutation energy. The circuit is simple

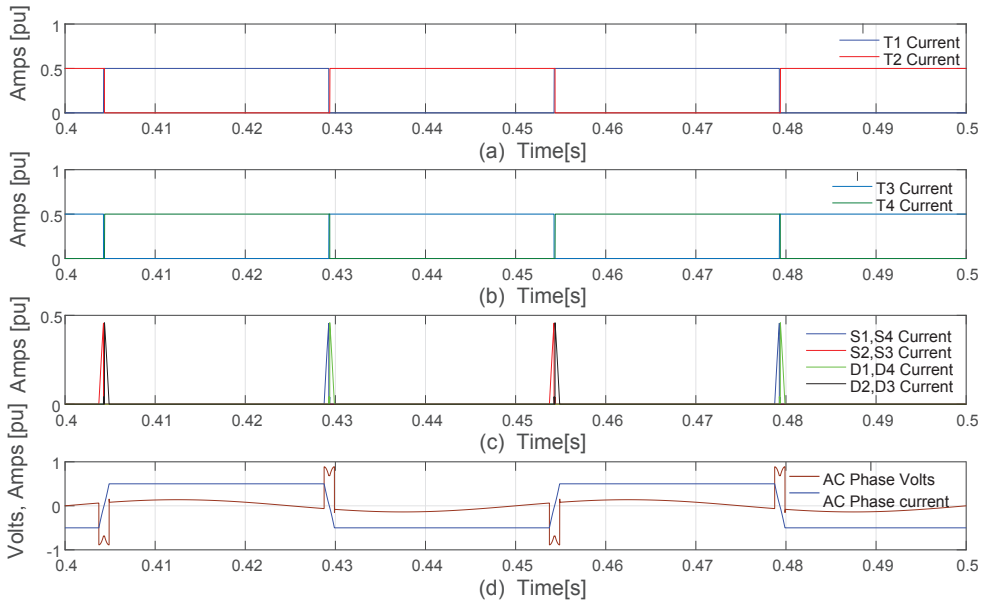

Fig. 4.40 H-bridge Energy Recovery Circuit: H-Bridge and Energy Recovery Circuit Volts and Amps.

and can be easily realised using IGBT or MOSFET H-bridge modules that are widely available commercially. Owing to the very short operating intervals of the clamping and energy recovery circuit relative to the non commutation time interval, the average energy handled by this circuit is relatively small, hence the rating of this circuit is minimal compared to that of the phase H-bridge converter cells.

In steady state, the amount of energy transferred from and absorbed by the clamp capacitor reaches an equilibrium balance, where the voltage across the clamp capacitor varies proportionally with load current & commutating inductance and is inversely proportional to time length of the energy recovery mode. A smaller energy recovery period results in an increased clamp capacitor dc link voltage. The duration of the energy recovery mode should be controlled to ensure that the clamp voltage is maintained with desired upper and lower limits. The upper limit is set to ensure the peak clamp voltage is still with the safe operating area of the H-bridge semiconductor devices and machine insulation voltage withstand rating. By applying energy conservation principle between the machine commutating inductance and clamp capacitor, the peak capacitor voltage can be expressed as;

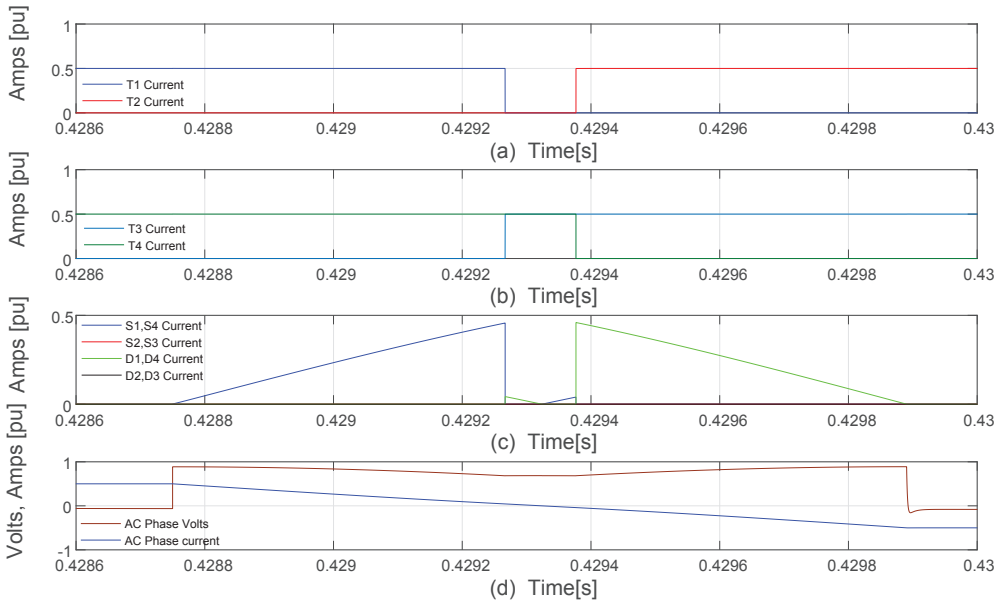

Fig. 4.41 H-bridge Energy Recovery Circuit: Commutation Interval; H-Bridge and Energy recovery Circuit Volts and Amps.

$$V_{C_{clamp}} = E_0 + \frac{I_{dc}}{2}\sqrt{\frac{L_c}{C_{clamp}}} \tag{4.38}$$

where, E_0 is the clamp capacitor voltage before energy transfer into capacitor, L_c is the machine phase commutating inductance and I_{dc} is the machine output dc link current.

The lower limit can be set to ensure the clamp capacitor voltage is always above the machine phase peak voltage under all operating conditions to avoid energy transfer from the machine into the clamp circuit during operating periods when no device commutation occur over the fundamental cycle.

4.7 Multi-Level Machine & Converter Integration

One key goal of this work is to study machine and converter topologies that lend themselves to full machine & converter physical integration as a single enclosure unit. Integration of the machine and drive provides a number of potential advantages, particularly at the system level. Some of these benefits include;

(a) Integrated drives makes it possible to reduce the total drive volume by eliminating the need for separate housings for the motor and drive controller electronics.

The integration eliminates cable runs between the converter and machine. This is desirable particularly for multiphase machines where the amount of cabling and consequential cabling cost can be significant.

(b) Integrating the power electronics in the machine housing also reduces the overall drive system weight.

(c) Eliminating cabling also facilitates reduction of Electromagnetic Interference, reduction of common mode currents and machine winding over voltages that can occur with long cables between converter and machine. This eases filtering requirements that would otherwise be required for long cable runs, yielding potential further cost reduction.

(d) Integration of machine and converter together with the multiphase approach can reduce the current and voltage stresses as the total drive power is distributed across multiple subunits.

(e) Reduction of overall drive system footprint. This is attractive for applications where space is a premium and small overall drive footprint is important.

(f) Potentially simplifies the cooling system since a common singular cooling system can be used for both machine and converter.

The benefits of machine and converter integration has been recognised as evidenced by increased research activities in machine and converter integration [145]. The multiphase/multilevel topologies presented in this work lend themselves very well to electromechanical integration of machine and converter as a single unit.

4.7.1 Applicable Power Electronic Switching Modules

As highlighted in section 2.9, the topology features a high number of stator phases. The Electronic Commutator devices switch at the machine fundamental frequency which is typically very low, 10 Hz up to 200 Hz range being envisaged. Owing to this low switching frequency, power electronic switching devices optimised for low conduction losses will be ideal since switching losses are minimal. Power electronic devices with, reverse voltage blocking capability (symmetric or asymmetric) and

gate assisted/controlled current turn off capability will be required. Whole wafer Thyristor type switching devices with gate assisted current commutation such as Gate Commutated Thyristors (GTO)and Integrated Gate-Commutated Thyristor (IGCT)are equally applicable to this topology. Other devices such as Insulated-Gate Bipolar Transistor (IGBT), Metal Oxide Semiconductor Field Effect Transistor (MOSFET)are equally applicable when used in series with reverse voltage blocking diodes.

As highlighted earlier for this multilevel machine and converter topology, low voltage devices with very low on-state Ohmic losses can yield potential significant efficiency improvement benefits. Recently IGBTs with reverse blocking capabilities have been reported in literature [146–151] and some manufacturers have started commercial production of these devices. Also, with recent advances in power semiconductor device and packaging technology, MOSFETs and normally off Junction Field Effect Transistors (JFETs) with very low on-state losses can now be realised [152], [153]. However, due to the reverse voltage blocking requirement for this machine and converter topology, MOSFETs & JFETS in their conventional packaging will not be suitable for this application. If however, the MOSFETs or JFETS can be repackaged with either series voltage blocking diodes or alternatively repackaged in a back to back configuration and operated in synchronous rectification mode, they can be utilised in this topology. This can potentially yield H-bridge cells with sufficiently low on-state losses, desired voltage blocking with inherent fault current limiting capability.

If silicon carbide MOSFET devices capable of operating at much higher junction temperatures [154–157] are employed, the H-bridge cells can be integrated as part of the machine, resulting in a very compact and power dense machine converter assembly. This is highly desirable for applications where space is a premium such as marine, offshore and aviation industries. This can potentially lead to reduced footprint of the overall drive system and consequently smaller overall power system plant. Moreover, the high thermal conductivity makes SiC an excellent candidate for harsh environments. However, there are still some significant challenges that have to be overcome before this technology can be commercially fully exploited for high temperature applications. These include:

Passive Components: In order to fully exploit the high temperature advantages of SiC devices, the passive auxiliary components required to realise a power electronic circuit such as gating electronic circuits, require passive components that are capable of operating at these high temperatures. These passive components include capacitors and wound magnetic components. Little attention has been paid to high temperature passive components that could enable the full SiC potential. More work is now being done to study, develop and fully characterise the performance of passive components for use in high temperature applications [158–161].

Device Packaging: Current semiconductor packaging has been adapted to the Si temperature limit of 175 degrees Celsius [154, 155] and is unsuitable, conventional plastic package cannot be exposed to such high temperatures. Further work is required in order produce SiC device packaging that is capable of dealing with the higher absolute junction temperatures and cope with higher temperature swings, thermal and power cycling duty. Research activities in semiconductor device packaging for high temperature applications is increasing [162–165] to enable exploitation of the advantages of wide band gap semiconductor devices.

Low Volume Cooling Systems: One key reason for wanting to operate at high ambient temperatures is that it can facilitate use of low volume cooling systems. However, device Junction temperatures exceeding 175 degrees Celsius can have a negative impact on converter efficiency due to the consequent rise in device losses with increasing temperature. Owing to the constraints in packaging and heat extraction from the devices, a tradeoff between losses and operating temperature may be required as the losses of SiC power semiconductors increase with device temperature, leading to a consequent decrease in converter efficiency [156, 166, 167, 145]. This general trade-off gives rise to an optimization procedure because the power, that can be dissipated by the cooling system, rises linearly with temperature while the losses typically show a steeper increase with temperature. That is, for a given converter at a certain temperature, the device current cannot be increased any more even though the junction temperature increases but must be decreased in order to prevent the device from a thermal

runaway [155]. However, with ongoing developments in high temperature operation of the power electronics components, heatsinking and active cooling thermal management strategies can be significantly downgraded, thus reducing the size, volume, and weight of the overall power electronic systems by as much as two orders of magnitude [154].

Cost: . Currently the cost of developing and applying devices and passive components for such high temperature environments is still prohibitive for commercial exploitation, but will decrease as these technologies become readily available [145].

4.7.2 Machine and converter Electromechanical Packaging

Electromechanical integration of machine and converter presents a number of challenges in terms of thermal management and mechanical packaging. The converter will require robust power electronic components and auxiliary control circuit components capable of withstanding the harsh environments typically required for machine and converter integration. The thermal demands of power electronic converters and electrical machines vary considerably due to the large heat flux of the power electronics compared to the machine. Typically machine stator windings (major heat source) operate at temperatures ranging from 150 to 200 degrees Celsius. Thermal limitations of existing silicon based power electronic devices and gating electronics components presents a barrier due to their inability to operate at typical ambient temperatures of electrical machine enclosures. A summary of the work reported in [168] on the operating temperature limits of main converter components is summarised in figure 4.42, note the figures for silicon exclude the device packaging temperature limits.

The machine and converter topologies considered in this work seek to facilitate machine and converter integration by addressing some of the key factors affecting the thermal management problem. The topologies seek to increase the converter efficiencies, hence reduce heat extraction challenge in a number of ways.

Firstly, the topologies employ devices that switch at machine fundamental frequencies that are typical low, less than 100 Hz as opposed to kHz switching frequencies of typical PWM controlled converters. This means power electronic devices can

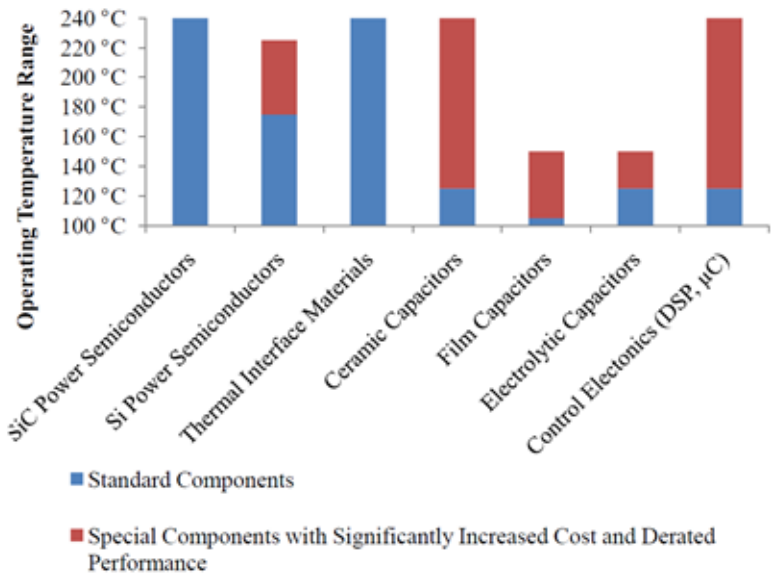

Fig. 4.42 Operating Temperatures Limitations of Main Converter Components.

be optimised for low conduction losses since switching losses are less significant. Secondly, the combination of multiphase machine and multilevel converter facilitates modular construction of the converter phase modules. Thirdly, the potential prospect of high temperature operating wide band gap devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) devices can operate at higher ambient temperatures and also offer reduced switching and conduction losses thereby easing the thermal integration requirements. Additionally, unlike the integrated drives presented in literature [148],[169, 170, 69, 171, 172, 145, 173] which have a power limit threshold in the kilowatt range, the topologies discussed here although they are applicable to low power systems, are primarily targeted at Megawatt power range machines with low fundamental base frequencies. In such machines, owing to their large physical size, there is sufficient space to integrate the phase switching modules, either surface mounting, axial mounting or modular segmented integration.

Segmented Modular Integration

Figure 4.43 shows a concept 3D model with the converter switching modules mounted on the end windings of the machine. The multiphase concept facilitates this modular integration of power electronic phase modules on the machine winding phase terminals. This integration arrangement is very desirable from commutating inductance

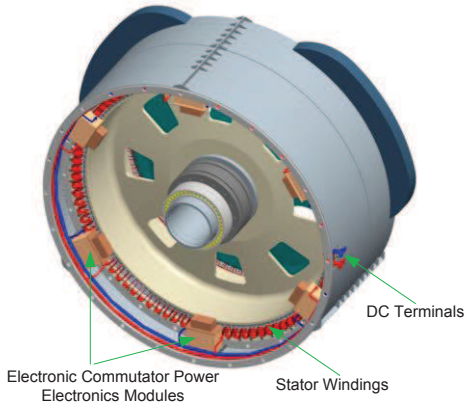

Fig. 4.43 Concept 3D Model concept of Machine & Phase Switching Modules Integration.

minimisation viewpoint and less coil end winding and cabling to power electronic phase modules is minimised. This modularised approach can yield compact high power density drives.

End Plate Integration

Figure 4.44 shows a concept another concept with the power electronics converter integrated on the non drive end of the machine. This configuration offers a stable and easily accessible mechanical platform for mounting power electronics. The power electronics can be packaged as modular withdrawable units that can be replaced and maintained easily.

Surface Mounted Integration

Figure 4.45 shows a three dimensional concept illustration of Multi-Megawatt machine with the converter integrated on the top surface of the machine housing. The power electronics is assembled in a hermetically sealed container which acts as a thermal barrier between the machine and the converter. The modular approach will enable integration of the phase switching modules with the machine to yield compact designs and eliminate cabling requirements between converter and machine. In this case only two cables for the dc terminals will be required from the drive to the dc power delivery system.

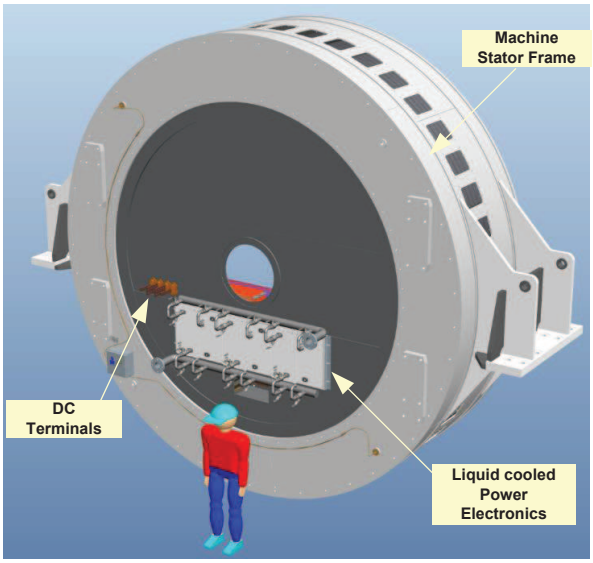

Fig. 4.44 Machine Converter Integration Concept With Liquid Cooled Power Electronics.

In the above mounting arrangements, forced air, liquid cooling systems, or a combination of both methods can be applied for cooling the integrated power electronics converter . The choice of which cooling system to apply will depend on the application requirements such as power level, footprint, cost, etc. With an ever increasing demand for high power density drives, the integration of machine and converters into a single housing remains attractive and warrants further research and development.

4.8 Summary

This chapter has introduced and discussed multilevel topologies suitable for multiphase current source converters. The multiphase approach enables the phase current to be reduced significantly for a given power level as the phase number increases. this facilitates machine design and manufacturing as smaller diameter wire can be used for the machine phase coils. It also eliminated the need for paralleling power electronic switching devices and the associated steady state and dynamic current sharing drawbacks. The multilevel approach enables commercially available low voltage semiconductor devices to be applied to high voltage high power machines without the need for series connection of several semiconductor devices in a phase arm, thereby

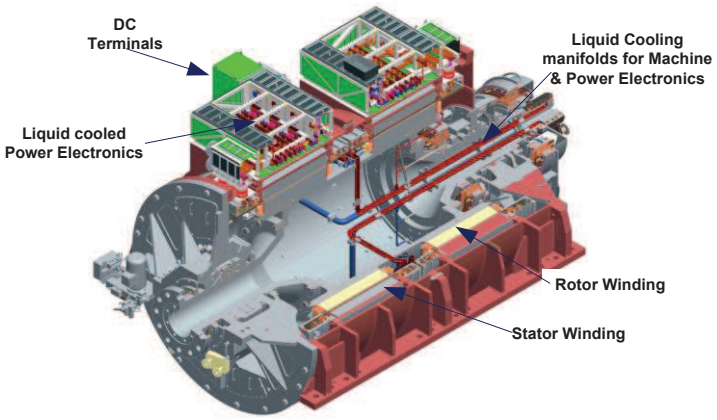

Fig. 4.45 Concept 3D Model of Machine with Integrated Power Electronics using Liquid Cooling for Both Machine and Power Electronics .

eliminating the steady state and dynamic voltage sharing drawbacks encountered with seriesed switching devices.

A combination of the multiphase and multilevel approach enables modularised power electronic switching phase modules to be realised, aiding machine-converter integration, manufacturing and maintenance of the drive system. The low semiconductor switching frequencies inherent in these drive topologies further improves the drive efficiency owing to the significant reduction in switching losses when compared to conventional PWM based drive topologies. Additionally, drive fault tolerance is enhanced if the machine stator phase number is sufficiently increased, resulting in improved drive availability. This is particularly desirable for applications where the drives are installed in harsh environments or harder to reach places where maintenance intervals are long, such as offshore or subsea applications. With technological advances in semiconductor device packaging and passive components for high temperature, the discussed drive topologies render themselves well to machine and converter integration into a single drive unit. The multilevel multiphase approach offers improved harmonic performance of the drive unit, leading to reduced passive filtering components and reduced drive torque pulsations.

One less attractive feature of multiphase multilevel drive topologies is the high semiconductor device could which can adversely affect the overall drive reliability. However, it should be borne in mind that regardless of the high phase number, for a

given drive VA rating, the overall drive semiconductor device VA rating is the same. In conventional PWM drives, often the high power rating is achieved by paralleling several converters per phase. In this approach, reliable smaller low voltage modular units can be designed and used to obtain drives with high reliability figures. The multilevel topology enables converter fed machines with very high dc link voltages to be realised using commercially off the shelf low voltage semiconductor modules. The use of widely available commercially off the shelf semiconductor modules can lead to further cost reduction.

Chapter 5

Modelling Of Multiphase Electronically Commutated DC Machine Topologies

5.1 Introduction

Physical models and test rigs have been widely used and continue to be used to de-risk and characterise the operational behaviour of new drive topologies. However, they can be prohibitively expensive depending on the scope, size and complexity of the drive systems being considered. Moreover, such systems pose a risk to personnel and equipment and offer limited capabilities in terms of characterising the behaviour of the system during non-linear events such as system faults. Therefore, it's imperative to develop models of sufficient fidelity to enable full characterisation of these systems via simulations. However, the modelling of machines with multiple power electronic convertors can be challenging owing to the highly non linear nature of the drive topology. Additionally, the choice of simulation program and modelling techniques play an important role since it has a direct bearing on the complexity, computational time and fidelity of the models.

A lot of research has been done in developing accurate machine simulation models for conventional 3 phase ac machines to enable the study and characterisation of their steady state and dynamic behaviour when connected to power electronic systems.

These machine models are also valuable for developing, studying and evaluating the suitability and performance of connected power electronic circuits and their associated control and protection strategies.

The machine topology being considered in this work departs from the conventional machines in a number of ways. Firstly, it consists of a significantly large number of stator phases, up to 24 or even higher. Secondly, both even and odd number of stator phases are applicable to this machine topology. Thirdly, the way in which the machine stator phases are connected and linked to external circuits is different. Unlike conventional machines where the stator phases are connected in series or parallel and in either star/delta connections on the ac side, in this machine topology each individual machine stator phase winding terminals are connected to a dedicated power electronic phase module as discussed in chapter 3 and chapter 4.

The multiphase electronically commutated DC machine topology, its multiphase windings and the associated power electronics topology represents a significant departure from the conventional machines and power circuit topologies currently in use such as, induction & synchronous machines with voltage and current source converters. As such, the generic machine simulation models developed so far and incorporated in commercial simulation packages do not lend themselves well to simulation studies of this machine/converter topology.

To enable transient, dynamic and steady state behaviour characterisation of this machine/converter topology and assessment of suitable power electronics and the protection strategies, suitable machine models have to be developed. This chapter details the machine modelling approach adopted for this machine & converter topology.

5.2 Modelling Approaches

A number of machine modelling methods have been proposed in literature [174–178, 171] and some are in wide use today. In order to determine the most suitable approach for modelling this machine topology, a review of the modelling approaches used for machine simulation models will be briefly highlighted. The four most applicable machine modelling approaches used in simulation of machine and converter systems are; (a) Finite Element modelling, (b) Phase domain machine modeling, (c)

DQ machine modelling and (d) Voltage behind reactance modelling. Each one of these methods has some key strengths and also some drawbacks depending on the intended purpose of the model.

Finite Element Modelling

Machine FE models are very accurate since they take into account the geometrical, material and operational details of electrical machine [179–181]. As a result, Finite Element methods are widely used in machine design stages. However, the intended purpose of the machine models in this work is for drive system dynamic behaviour prediction to facilitate the detailed design of the drive system, where not only the electric machine is included, but also the power electronics and control systems that interact with it. Owing to the need to calculate the machine parameters at each time step, the computational requirements of time stepping 2 & 3 dimensional FE simulations are very high. The computational burden coupled with the FE modelling complexity renders this approach less suitable for modelling such a drive system.

Phase Domain Modelling

In this formulation, the machine is represented in its natural form by lumped parameter coupled circuits in physical variables and abc phase coordinates. This modelling approach lends itself well to simulation of machines connected to power electronic circuits as machine circuits are directly inserted into the overall system circuit network equations, thus providing a simultaneous solution. Owing to this integration of the machine model with the rest of the power electronic system, the machine converter system behaviour during certain machine/converter failure modes such as open or short circuit faults can be readily simulated. Various academic publications [174, 182–185] have shown that this machine modelling approach improves numerical accuracy and stability of the system being simulated. In this formulation, the stator inductances are rotor position dependent and will have to be computed at each rotor position. Furthermore, the inversion of the inductance matrix is required at each time step during the numerical integration of the differential equations as the rotor changes position. This imposes a heavy computational burden during simulation particularly

if the size of this matrix is large, as is the case with multi phase machine topology being considered. For machines with relatively low number of phases, this drawback can be mitigated by computing analytical expression of the inductance matrix inverse offline either by hand calculations or using symbolic maths software packages such as Mathematica and implementing the resultant simplified equations in the machine models. Work has also been reported in literature ([186], [187], [186]) where block matrix inversion techniques exploiting the circulant nature of the submatrices such that inductance matrix inversion is avoided. Instead, analytical expressions of submatrices of the inverse of the inductance matrix are used [188],[189]. However, all these techniques become tedious and error prone when significantly high number of phases are considered.

DQ Modelling

The *dq*-machine modelling formulations have gained wide acceptance in many nodal analysis-based electromagnetic transient programs (EMTP-type) and state variable-based simulation programs (e.g., Simulink, PLECS e.t.c.) as built-in standard library components that are extensively used both in industry and academia. This formulation is based on the transformation of machine variables into an imaginary reference frame, the so called *dq* Park transformations. With *dq* transformation, the sinusoidal machine variables (volts, currents, fluxes) are transformed into DC quantities. This is quite attractive from a computational overhead viewpoint as it results in a constant steady state matrix of self and mutual inductances (i.e. inductances are independent of rotor position). Thus, in the machine model implementation the inductance matrix does not need to be recalculated at each simulation time step as the rotor changes position, making it numerically efficient. However, this method does not lend itself well to the simulation of the machine/converter topology proposed (machine and associated power electronics) for the following reasons. Prediction of a number of variables is required to interface the *dq* circuits of the model with the phase-domain representation of the power electronic circuit being simulated. A number of methods are used to interface the *dq* machine model to the rest of the system circuits. These include; use of a Norton equivalent in phase coordinates where the Norton resistance matrix is approximated

to become time-independent and the Norton current sources is computed from the *dq* model. Alternatively, a compensation method in which the main machine stator circuit is represented by a Thevenin equivalent circuit and interfaced to the *dq* circuits can be used. However this is limited to a number of topologies. A third approach used is to interface the machine *dq* model with the stator circuit as a compensated current source with special terminating resistance. The Norton current source that represents the machine is calculated using the previous time point terminal voltages of the machine. These interface methods often cause deterioration of numerical accuracy if larger time steps are used and often small time steps are required to keep interfacing errors within required tolerances. In some cases, this can lead to stability issues of the overall system. Often, terminating impedances / snubber circuits are needed at the machine terminals to aid numerical stability and facilitate integration with the rest of the power circuit. Furthermore, representation of the machine internal phenomenon such as short circuits and more importantly, the machine behaviour during electronic commutation process and system faults is somewhat difficult. This is particularly important in this drive topology where the power electronic modules are an integral part of the machine phases and can not be decoupled when studying the behaviour of this machine during normal and faulty operating conditions.

Voltage Behind Reactance Modelling

Recent studies have also proposed alternative approaches based on Voltage Behind Reactance (**VBR**) modelling for electrical machines [190–197]. In this approach, the machine equations are reformulated such that the machine rotor subsystem dynamics are decoupled from the stator subsystem dynamics. Here, the rotor subsystem dynamics are represented using state variable equations in the *dq* coordinate system whereas the stator subsystem dynamics are represented in circuit form in the *abc* phase coordinate system. Reformulating the machine equations in this way brings several advantages, particularly in drive system simulations where the machine is integrated as part of a power electronic system network.

Since the machine stator subsystem is represented in the physical *abc* phase domain with voltages behind lumped impedances (inductive & resistive), it naturally lends

itself well for direct interfacing to the rest of the power electronic system network as its typically represented in the *abc* phase coordinates. This also circumvents the machine variables predictions/iterations interface problems encountered in the *dq* model formulations, thereby improving the numerical stability of the simulated system. In comparison to the phase domain formulation, the implementation of the rotor subsystem in *dq* coordinates gives improved computational overhead and also inductance matrix inversion is avoided. Additionally, with machines where the stator and rotor time constants are orders of magnitude apart, the decoupling of the stator and rotor dynamics in this formulation affords the use of multi-rate simulations where different time-steps can be applied for the stator and rotor subsystems during simulations. Furthermore, the natural interface of the stator subsystem with the rest of the power electronic circuit means that the internal machine/converter fault conditions can be fully characterised. However, the voltage behind reactance formulation is numerically less efficient in comparison to the *dq* formulation due to the rotor position dependent inductances. Inspite of this increased computational overhead, this formulation is quite attractive for the machine topology being considered owing to the above mentioned advantages. Moreover, with the recent technological developments in computer hardware, reasonable simulation times can be attained with today's standard computer hardware. This work aims to extends the VBR modelling formulation to the multiphase electronically commutated DC machine topology.

5.3 Voltage Behind Reactance Modelling

Without loss of generality, an *n*-phase machine with symmetrical and sinusoidally distributed stator windings is considered. It is assumed all the stator phase winding terminals are available for connection to the associated power electronic circuits. The rotor is represented by a lumped *RL* circuits with multiple *qd*- axis damper windings and one field winding. The motor convention will be used henceforth. Figure 5.1 shows an illustration of the model formulation and partition between the stator and rotor subsystems.

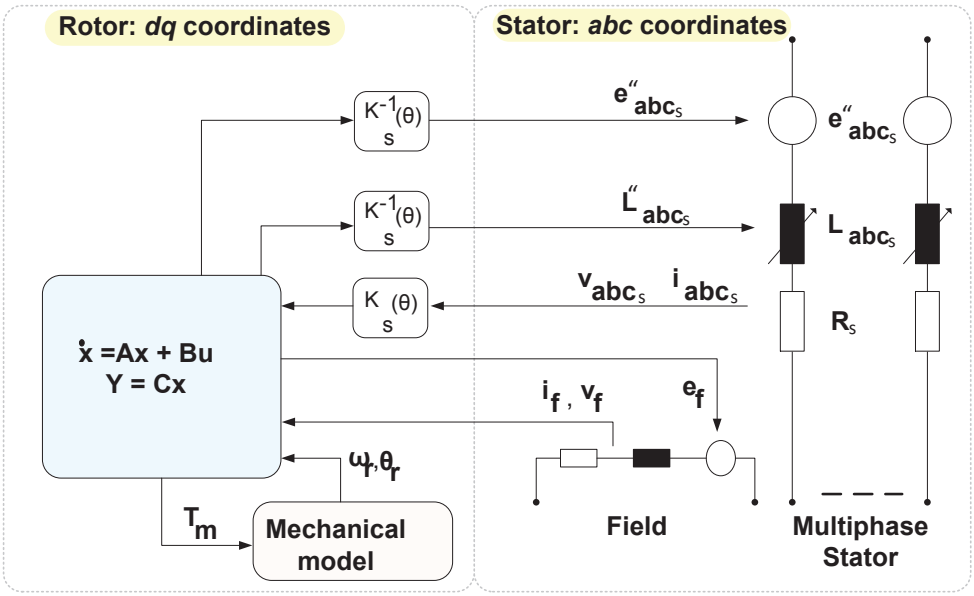

Fig. 5.1 Representation of the Voltage Behind Reactance Model Formulation

5.3.1 Voltage Behind Reactance Formulation

As alluded to earlier, the **VBR** formulation represents the stator variables in the *abc* phase coordinates and the rotor in the *dq*-frame coordinates. For the machine topology being considered, electronic commutation is an integral part for the operation of the machine. The electronic commutation process is significantly influenced by the sub-transient characteristics of the machine. As such, the **VBR** formulation lends itself well for simulation studies of the machine electronic commutation process and such a model will facilitate the design and performance characterisation of the phase power electronic modules. In this **VBR** formulation, the stator voltage equation is expressed in general form as:

$$v_{abc_s} = R_s i_{abc_s} + \frac{d}{dt}\left[L''_{abc_s}(\theta_r) i_{abc_s}\right] + e''_{abc_s} \tag{5.1}$$

where v_{abc_s} and i_{abc_s} denote the stator voltages and currents, θ_r is the rotor electrical angle, L''_{abc_s} is a variable inductance matrix which is a function of the rotor position and the voltage e''_{abc_s} represents the voltage vector linking the rotor subsystem to the stator circuit. In this formulation, (8.12) defines the interfacing circuit to the rest of the system power electronics network.

In this chapter, the derivation of the stator and rotor subsystem equations will be described. Its worth highlighting at this stage that the formulation derived here is targeted for implementation in a state variable based transient simulation program such as Matlab/Simulink or Piece-wise Linear Electrical Circuit Simulation (**PLECS**).

5.3.2 Rotor Subsystem

The rotor sub-system state equations can be represented in the generic state-space form as:

$$\frac{d}{dt}x = \mathbf{A}x + \mathbf{B}u \tag{5.2}$$

$$y = \mathbf{C}x \tag{5.3}$$

where the x is the system state variables vector and u is the input variables vector which can represent input currents and voltages, y is the output vector and the matrices **A**, **B** and **C** are the, system matrix describing the internal dynamics, input matrix and the output matrix respectively.

Rotor d-axis State Equations

Although the final model implemented in the simulation work assumes only one d-axis damper winding, for completeness, a generalised formulation covering machines with more than one damper winding will be presented here. The d-axis rotor state space equations can be formulated as shown below, assuming the machine has m d-axis windings. It is assumed the d-axis windings comprise of one field winding and multiple damper windings. In this analysis, all the rotor variables are not referred to the stator, i.e. the unreferred rotor physical variables e.g. the actual rotor field voltages and currents are used.

Choosing the rotor winding flux linkages as state variables with rotor voltages as inputs and rotor currents as outputs, the rotor subsystem can be expressed in state space form as:

$$\frac{d}{dt}\begin{bmatrix}\lambda_{fd}\\ \lambda_{kd1}\\ \lambda_{kd2}\\ .\end{bmatrix} = \begin{bmatrix}-\frac{r_{fd}}{L_{fd}} & 0 & 0 & .\\ 0 & -\frac{r_{kd1}}{L_{kd1}} & 0 & .\\ 0 & 0 & -\frac{r_{kd2}}{L_{kd2}} & .\\ . & . & . & .\end{bmatrix}\begin{bmatrix}\lambda_{fd}\\ \lambda_{kd1}\\ \lambda_{kd2}\\ .\end{bmatrix} + \begin{bmatrix}1 & -1\\ 1 & 0\\ 1 & 0\\ . & .\end{bmatrix}\begin{bmatrix}v_{md}\\ v_{fd}\end{bmatrix} \tag{5.4}$$

In the formulation presented herein, the following notations shall be used to represent machine parameters: *kq, kd* represent the *qd* damper windings, *fd* represent the field winding, λ represent flux linkage; *qs* & *ds* represent stator *qd* variables, v_{md} is the magnetising branch voltage, *qr* & *dr* represent rotor *qd* variables respectively and ω_r & θ_r are the rotor angular speed and position respectively and the subscript numbers $1,2$ represent damper winding circuit numbers. Figure 5.2 shows a schematic diagram of the *dq* circuits.

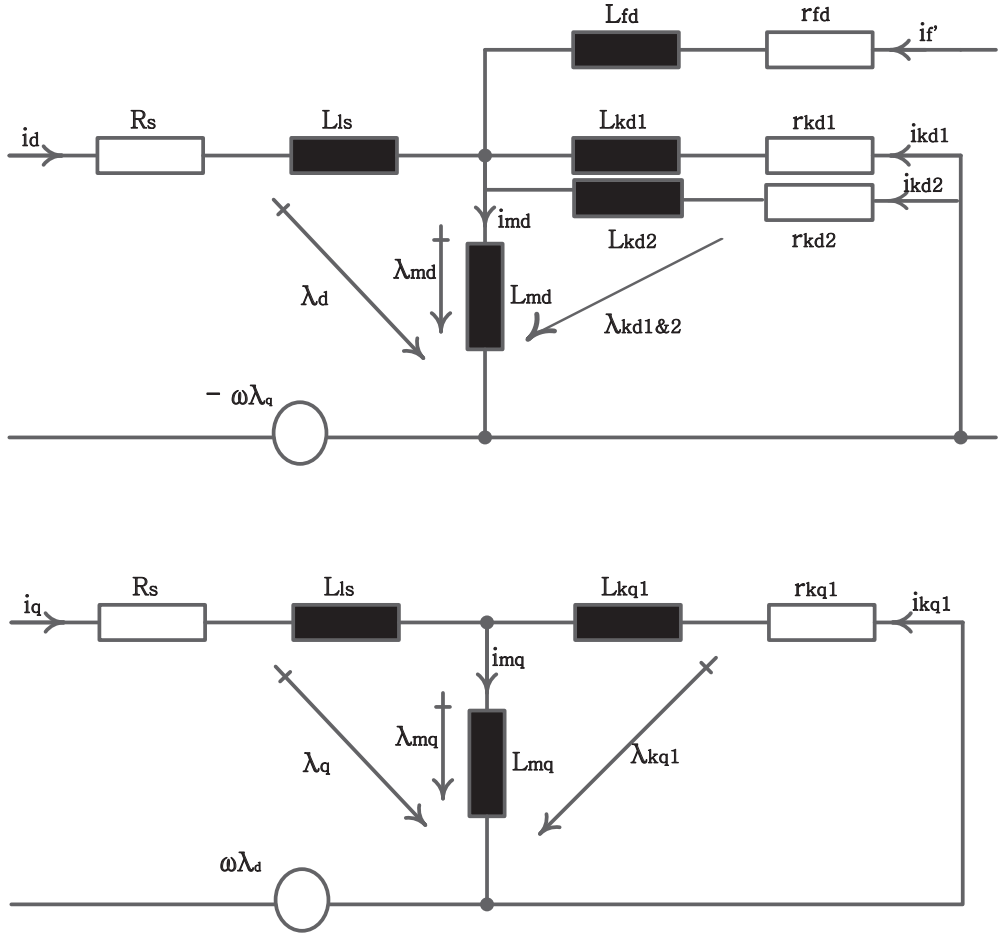

Fig. 5.2 Representation of the Machine *dq* Equivalent Circuits

$$\begin{bmatrix} i_{dr} \\ i_{fd} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_{fd}} & \frac{1}{L_{kd1}} & \frac{1}{L_{kd2}} & . \\ \frac{1}{L_{fd}} & 0 & 0 & . \end{bmatrix} \begin{bmatrix} \lambda_{fd} \\ \lambda_{kd1} \\ \lambda_{kd2} \\ . \end{bmatrix} \tag{5.5}$$

Similar to the analysis presented in [197], some internal d-axis rotor network state variables can be defined so that the derivatives of the d-axis state variables in (5.4) dependent on the d-axis rotor flux linkages instead of their derivatives. The rotor network internal state vector y_d can defined as:

$$[y_d] = \begin{bmatrix} y_{d1} \\ y_{d2} \\ . \end{bmatrix} \text{ such that: } \begin{bmatrix} \lambda_{fd} \\ \lambda_{kd1} \\ \lambda_{kd2} \\ . \end{bmatrix} = [y_d] + \begin{bmatrix} 1 \\ 1 \\ 1 \\ . \end{bmatrix} [\lambda_{md}] \tag{5.6}$$

i.e.

$$\begin{bmatrix} \lambda_{fd} \\ \lambda_{kd1} \\ \lambda_{kd2} \\ \vdots \end{bmatrix} = [y_d] + \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \end{bmatrix} [\lambda_{md}] \tag{5.7}$$

Substituting (5.7) in (5.4) & rearranging using ($v_{md} = \frac{d}{dt}\lambda_{md}$) and grouping terms gives:

$$\frac{d}{dt}[y_d] = \begin{bmatrix} \frac{-r_{fd}}{L_{fd}} & 0 & 0 & . \\ 0 & \frac{-r_{kd1}}{L_{kd1}} & 0 & . \\ 0 & 0 & \frac{-r_{kd2}}{L_{kd2}} & . \\ . & . & . & . \end{bmatrix} [y_d] + \begin{bmatrix} \frac{-r_{fd}}{L_{fd}} & -1 \\ \frac{-r_{kd1}}{L_{kd1}} & 0 \\ \frac{-r_{kd2}}{L_{kd2}} & 0 \\ . & . \end{bmatrix} \begin{bmatrix} \lambda_{md} \\ v_{fd} \end{bmatrix} \tag{5.8}$$

Expressing the rotor current i_{dr} in (5.5) in terms of this new rotor state vector y_d gives:

$$\begin{bmatrix} i_{dr} \\ i_{fd} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_{fd}} & \frac{1}{L_{kd1}} & \frac{1}{L_{kd2}} & . \\ \frac{-1}{L_{fd}} & 0 & 0 & . \end{bmatrix} \begin{bmatrix} [y_d] + \begin{bmatrix} 1 \\ 1 \\ 1 \\ . \end{bmatrix} [\lambda_{md}] \end{bmatrix} \tag{5.9}$$

The derivative of the rotor d-axis & field current i_{fd} is given by differentiating (5.9) above with respect to time and substituting (5.8) to give:

$$\frac{d}{dt}\begin{bmatrix} i_{dr} \\ i_{fd} \end{bmatrix} = \begin{bmatrix} \frac{-r_{fd}}{L_{fd}^2} & \frac{-r_{kd1}}{L_{kd1}^2} & \frac{-r_{kd2}}{L_{kd2}^2} & . \\ \frac{r_{fd}}{L_{fd}^2} & 0 & 0 & . \end{bmatrix} [y_d] + \begin{bmatrix} -(\frac{r_{fd}}{L_{fd}^2} + \frac{r_{kd1}}{L_{kd1}^2} + \frac{r_{kd2}}{L_{kd2}^2} + .) & \frac{-1}{L_{fd}} \\ \frac{r_{fd}}{L_{fd}^2} & \frac{1}{L_{fd}} \end{bmatrix} \begin{bmatrix} \lambda_{md} \\ v_{fd} \end{bmatrix} + \begin{bmatrix} (\frac{1}{L_{fd}} + \frac{1}{L_{kd1}} + \frac{1}{L_{kd2}} + .) \\ -\frac{1}{L_{fd}} \end{bmatrix} \frac{d}{dt}[\lambda_{md}] \tag{5.10}$$

Expressing the field current derivative term of (5.10) in terms of the field voltage v_{fd} gives:

$$v_{fd} = \begin{bmatrix} \frac{-r_{fd}}{L_{fd}} & 0 & 0 & . \end{bmatrix} [y_d] - \frac{r_{fd}}{L_{fd}}\lambda_{md} + L_{fd}\frac{d}{dt}i_{fd} + \frac{d}{dt}\lambda_{md} \tag{5.11}$$

Substituting (5.11) in the rotor current derivative equation (5.10) to eliminate v_{fd} and simplifying and grouping terms gives:

$$\frac{d}{dt}i_{rd} = \begin{bmatrix} 0 & \frac{-r_{kd1}}{L_{kd1}^2} & \frac{-r_{kd2}}{L_{kd2}^2} & . \end{bmatrix} [y_d] - (\frac{r_{kd1}}{L_{kd1}^2} + \frac{r_{kd2}}{L_{kd2}^2} + .)\lambda_{md} + (\frac{1}{L_{kd1}} + \frac{1}{L_{kd2}}.)\frac{d}{dt}\lambda_{md} - \frac{d}{dt}i_f d \tag{5.12}$$

Rotor q-axis State Equations

A similar formulation to that presented for the rotor d axis subsystem will be carried out for the q-axis to generate the corresponding state space equations. Again for generality, it is assumed the rotor q axis has multiple (n) damper windings. The q-axis rotor state space equations can be formulated in matrix form as:

$$\frac{d}{dt}\begin{bmatrix} \lambda_{kq1} \\ \lambda_{kq2} \\ . \end{bmatrix} = \begin{bmatrix} -\frac{r_{kq1}}{L_{kq1}} & 0 & . \\ 0 & -\frac{r_{kq2}}{L_{kq2}} & . \\ . & . & . \end{bmatrix}\begin{bmatrix} \lambda_{kq1} \\ \lambda_{kq2} \\ . \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ . \end{bmatrix}\begin{bmatrix} v_{mq} \end{bmatrix} \tag{5.13}$$

with output q axis rotor current equation as:

$$\begin{bmatrix} i_{qr} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_{kq1}} & \frac{1}{L_{kq2}} & . \end{bmatrix}\begin{bmatrix} \lambda_{kq1} \\ \lambda_{kq2} \\ . \end{bmatrix} \tag{5.14}$$

Conducting a similar analysis on the q-axis rotor network to that done for the d-axis (5.6) - (5.8), a new internal state vector y_q can be defined as:

$$[y_q] = \begin{bmatrix} y_{q1} \\ y_{q2} \\ . \end{bmatrix} \quad \text{such that:} \quad \begin{bmatrix} \lambda_{kq1} \\ \lambda_{kq2} \\ . \end{bmatrix} = [y_q] + \begin{bmatrix} 1 \\ 1 \\ . \end{bmatrix}\begin{bmatrix} \lambda_{mq} \end{bmatrix} \tag{5.15}$$

Substituting (5.15) into (5.13) and grouping terms gives:

$$\frac{d}{dt}[y_q] = \begin{bmatrix} -\frac{r_{kq1}}{L_{kq1}} & 0 & . \\ 0 & -\frac{r_{kq2}}{L_{kq2}} & . \\ . & . & . \end{bmatrix}[y_q] + \begin{bmatrix} \frac{-r_{kq1}}{L_{kq1}} \\ \frac{-r_{kq2}}{L_{kq2}} \\ . \end{bmatrix}\begin{bmatrix} \lambda_{mq} \end{bmatrix} \tag{5.16}$$

Expressing the rotor current i_{qr} (5.14) in terms of y_q gives:

$$i_{qr} = \begin{bmatrix} \frac{1}{L_{kq1}} & \frac{1}{L_{kq2}} & . \end{bmatrix}\left[[y_q] + \begin{bmatrix} 1 \\ 1 \\ . \end{bmatrix}\begin{bmatrix} \lambda_{mq} \end{bmatrix} \right] \tag{5.17}$$

Using (5.16), the derivative of the rotor q-axis current is given by differentiating (5.17) above with respect to time to give:

$$\frac{d}{dt}i_{qr} = \begin{bmatrix} -\frac{r_{kq1}}{L_{kq1}^2} & -\frac{r_{kq2}}{L_{kq2}^2} & . \end{bmatrix} [y_q] - (\frac{r_{kq1}}{L_{kq1}^2} + \frac{r_{kq2}}{L_{kq2}^2}.)\lambda_{mq} + (\frac{1}{L_{kq1}} + \frac{1}{L_{kq2}}.)\frac{d}{dt}\lambda_{mq} \quad (5.18)$$

The equations presented above can be applied for simulating machines with any number of *qd* damper windings. The rotor *qd* current equations and their derivatives can be easily inferred from the above generalised equations by considering matrix elements up to the correct number of damper windings. For example, for a machine with two *q*-axis damper windings and one *d*-axis field winding and one *d*-axis damper winding, the derivative of the *qd*-axis currents become:

$$\frac{d}{dt}i_{qr} = \begin{bmatrix} -\frac{r_{kq1}}{L_{kq1}^2} & -\frac{r_{kq2}}{L_{kq2}^2} \end{bmatrix} \begin{bmatrix} y_{q1} \\ y_{q2} \end{bmatrix} - (\frac{r_{kq1}}{L_{kq1}^2} + \frac{r_{kq2}}{L_{kq2}^2})\lambda_{mq} + (\frac{1}{L_{kq1}} + \frac{1}{L_{kq2}})\frac{d}{dt}\lambda_{mq} \quad (5.19)$$

$$\frac{d}{dt}i_{rd} = \begin{bmatrix} 0 & \frac{-r_{kd1}}{L_{kd1}^2} \end{bmatrix} \begin{bmatrix} y_{d1} \\ y_{d2} \end{bmatrix} - \frac{r_{kd1}}{L_{kd1}^2}\lambda_{md} + \frac{1}{L_{kd1}}\frac{d}{dt}\lambda_{md} - \frac{d}{dt}i_fd \quad (5.20)$$

To simplify the ensuing formulation, block matrices (from matrix algebra,[186]) **A, B, C, D** can be defined such that rotor current derivatives (5.12) and (5.18) are combined and expressed in matrix form as:

$$\frac{d}{dt}\begin{bmatrix} i_{qr} \\ i_{dr} \end{bmatrix} = [\mathbf{A}_{[2\times(n+m)]}] \begin{bmatrix} y_{q_{[n\times1]}} \\ y_{d_{[m\times1]}} \end{bmatrix} + [\mathbf{B}_{[2\times2]}] \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} + [\mathbf{C}_{[2\times2]}]\frac{d}{dt}\begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} + [\mathbf{D}_{[2\times1]}]\frac{d}{dt}i_{fd} \quad (5.21)$$

where *n* & *m* represent the number of *qd* machine rotor windings respectively. The block matrices are partitioned to show the *qd* sub-matrices as highlighted below:

$$\mathbf{A} = \begin{bmatrix} A_{q_{[2\times n]}} & A_{d_{[2\times m]}} \end{bmatrix} \quad (5.22)$$

$$\mathbf{B} = \begin{bmatrix} B_{q_{[2\times1]}} & B_{d_{[2\times1]}} \end{bmatrix} \tag{5.23}$$

$$\mathbf{C} = \begin{bmatrix} C_{q_{[2\times1]}} & C_{d_{[2\times1]}} \end{bmatrix} \tag{5.24}$$

$$\mathbf{D} = \begin{bmatrix} D_{q_{[1\times1]}} \\ D_{d_{[1\times1]}} \end{bmatrix} \tag{5.25}$$

and the elements of the sub-matrices **A** to **D** are defined in Appendix A. The square bracketed numbers in the matrices indicate the size of the matrices and will be omitted in the following analysis.

Thus, the derivatives of the *qd* rotor currents equations become:

$$\frac{d}{dt}\begin{bmatrix} i_{qr} \\ i_{dr} \end{bmatrix} = [\mathbf{A}]\begin{bmatrix} y_q \\ y_d \end{bmatrix} + [\mathbf{B}]\begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} + [\mathbf{C}]\frac{d}{dt}\begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} + [\mathbf{D}]\frac{d}{dt}i_{fd} \tag{5.26}$$

5.3.3 Stator Subsystem

In this VBR formulation, the stator subsystem voltages and currents will be taken as inputs and the magnetising flux linkage vectors (λ_{md} & λ_{mq}) will be taken as state variables along with the defined internal rotor state vectors y_{qd}. For generality, it is assumed the machine model being formulated has N stator phases. The stator voltage equation can be expressed as:

$$[v_{abc..N_s}] = [r_s][i_{abc..N_s}] + \frac{d}{dt}[\lambda_{abc..N_s}] \tag{5.27}$$

where $v_{abc..N_s}$ and $i_{abc..N_s}$ are $N \times 1$ matrices whose elements are stator voltages & currents. The stator resistance matrix is an $N \times N$ diagonal matrix whose diagonal elements are the stator phase winding resistances (r), i.e. $r_s = r\mathbf{I}_{N\times N}$.

Stator Variables Transformation

The stator variables (voltages, currents, flux linkages) can be transformed to the rotor reference frame using an appropriate transformation matrix [198], [199]. Since this

work focuses on machines with a large number of stator phases (greater than the typical three phase), a generalised transformation matrix for machines with a high number of phases will be applied. As stated earlier, it is assumed the machine has N stator phase windings which are symmetrically distributed around the stator and offset from each other by $\alpha = \frac{2\pi}{N}$ radians.

The stationary stator variables denoted here by $\mathbf{f}$ (representing either the stator voltages, currents or flux linkages) are first transformed to a stationary *alpha - beta* reference frame by the transformation matrix T_2 given by:

$$[\mathbf{T_2}] = \frac{2}{N}\begin{bmatrix} \cos(\alpha.0) & \cos(\alpha.1) & \cdots & \cos(\alpha.(N-1)) \\ & & & \\ \sin(\alpha.0) & \sin(\alpha.1) & \cdots & \sin(\alpha.(N-1)) \end{bmatrix} \tag{5.28}$$

Its worth noting that a number of possible transformations are applicable and in use [32], [199], [200]. For example the so called power invariant transformation where the power and torque calculated by the *dq* variables are the same as those calculated by the *n* phase variables can be applied. However, the peak values of the *qd* variables are not the same as their corresponding stator counterparts. The transformation chosen for this work ensures the peak magnitude of the *dq* variables are the same as those of the corresponding N phase variables. In this transformation however, the power and torque calculated by the *dq* variables is smaller by a factor of $2/N$ compared to those computed by the corresponding phase variables. This is called the magnitude invariant transformation, and its advantages over the power invariant transformation are highlighted in [188]. Park's transformation can then be applied to the matrix T_2 to give the *dq* transformation matrix $\check{K}_s$ as follows:

$$[\check{\mathbf{K}}_s(\theta_r)] = [\mathbf{P}_s(\theta_r)][\mathbf{T_2}] \tag{5.29}$$

where the Park transformation matrix $P_s(\theta_r)$ is given by:

$$\mathbf{P}_s(\theta_r) = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{5.30}$$

The stator variables transformed into the rotor reference frame are now given by:

$$\left[\mathbf{f}_{qd_s}\right] = [\check{\mathbf{K}}_s(\theta_r)][\mathbf{f}_{abc..n_s}] \tag{5.31}$$

The transformed variables can be expressed in matrix form as :

$$\left[f_{qd_s}\right] = [f_{qs} \quad f_{ds}]^T \quad \& \quad [f_{abc..n_s}] = [f_{a_s} \quad f_{b_s} \quad .. \quad f_{n_s}]^T \tag{5.32}$$

where T denotes matrix transpose.

The magnitude invariant transformation $\check{K}_s(\theta_r)$ has some attractive attributes which will be exploited to simplify the analysis in the following sections. These include:

$$\check{\mathbf{K}}_s(\theta_r)\frac{d}{dt}[\check{\mathbf{K}}_s(\theta_r)]^{-1} = \begin{bmatrix} 0 & -\omega_r \\ \omega_r & 0 \end{bmatrix} \tag{5.33}$$

$$\frac{d}{dt}[\check{\mathbf{K}}_s(\theta_r)]\check{\mathbf{K}}_s(\theta_r)^{-1} = \begin{bmatrix} 0 & \omega_r \\ -\omega_r & 0 \end{bmatrix} \tag{5.34}$$

where the inverse of the transformation matrix can be readily computed using:

$$\check{\mathbf{K}}_s(\theta_r)\check{\mathbf{K}}_s(\theta_r)^{-1} = [\mathbf{I}]. \tag{5.35}$$

where $[\mathbf{I}]$ is an identity matrix.

In the machine topologies being considered, all machine phases are either directly or indirectly connected to one another through the power electronic circuits to form a polygonal winding. As such, no stator neutral point exists, and consequently no zero sequence current can flow from the machine to the connected system. As a result the zero sequence component terms are omitted in the analysis presented here.

Transformed *qd* Stator Variables

The *qd* transformed stator voltage equations can be expressed in the rotor reference frame as:

$$v_{q_s} = r_s i_{q_s} + \omega_r \lambda_{d_s} + \frac{d}{dt}\lambda_{q_s}; \quad \& \quad v_{d_s} = r_s i_{d_s} - \omega_r \lambda_{q_s} + \frac{d}{dt}\lambda_{d_s} \tag{5.36}$$

Using Kirchhoff's current law on the generic *qd* circuit representation similar to that presented earlier in figure 5.2 , the stator subsystem *qd* currents can be expressed as:

$$i_{qs} = i_{mq} + i_{qr}; \quad \& \quad i_{ds} = i_{md} + i_{dr} \tag{5.37}$$

Similarly, the stator flux linkages can be expressed in rotor reference frame as:

$$\lambda_{q_s} = L_{ls} i_{q_s} + \lambda_{mq}; \quad \& \quad \lambda_{d_s} = L_{ls} i_{d_s} + \lambda_{md} \tag{5.38}$$

where L_{ls} denotes the stator leakage inductance. Substituting (5.38) into (5.36) and rearranging and expressing in matrix form gives the stator voltage equations as:

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = r_s \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \omega_r L_{ls} \begin{bmatrix} i_{ds} \\ -i_{qs} \end{bmatrix} + \omega_r \begin{bmatrix} \lambda_{md} \\ -\lambda_{mq} \end{bmatrix} + L_{ls} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} \tag{5.39}$$

Differentiating the *qd* stator current (5.37) and expressing in matrix form gives :

$$\frac{d}{dt} \begin{bmatrix} i_{mq} \\ i_{md} \end{bmatrix} = \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} - \frac{d}{dt} \begin{bmatrix} i_{qr} \\ i_{dr} \end{bmatrix} \tag{5.40}$$

The derivatives of the magnetising flux linkage vector can be expressed as:

$$\frac{d}{dt} \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} = \mathbf{L_{\check{mqd}}} \frac{d}{dt} \begin{bmatrix} i_{mq} \\ i_{md} \end{bmatrix} \tag{5.41}$$

where $L_{\check{mqd}}$ is a *qd* magnetising inductance matrix. If machine saturation effects are neglected, this matrix is a diagonal matrix whose diagonal elements are the constant *qd* magnetising inductances L_{mq} and L_{md}. If saturation and salience effects are to be accounted for, a generalised symmetric *qd* magnetising inductance matrix can be formulated and represented as:

$$\mathbf{L_{\check{mqd}}} = \begin{bmatrix} L_{\check{mq}} & L_{\check{mqd}} \\ L_{\check{mqd}} & L_{\check{md}} \end{bmatrix} \tag{5.42}$$

where the superscript ˇ is used to denote the variable saturated inductance values.

Substituting (5.40) into (5.41) and rearranging gives:

$$\frac{d}{dt}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} = \mathbf{L}_{\mathbf{mqd}}\check{}\frac{d}{dt}\begin{bmatrix}i_{qs}\\ i_{ds}\end{bmatrix} - \mathbf{L}_{\mathbf{mqd}}\check{}\frac{d}{dt}\begin{bmatrix}i_{qr}\\ i_{dr}\end{bmatrix} \tag{5.43}$$

The rotor current derivative terms in (5.43) can now be eliminated by substituting the equation of the rotor current derivative (5.21) into (5.43) to yield:

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} = \mathbf{L}_{\mathbf{mqd}}\check{}\frac{d}{dt}\begin{bmatrix}i_{qs}\\ i_{ds}\end{bmatrix} - \mathbf{L}_{\mathbf{mqd}}\check{}\mathbf{A}\begin{bmatrix}y_q\\ y_d\end{bmatrix} - \mathbf{L}_{\mathbf{mqd}}\check{}\mathbf{B}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix}\\ -\mathbf{L}_{\mathbf{mqd}}\check{}\mathbf{C}\frac{d}{dt}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} - \mathbf{L}_{\mathbf{mqd}}\check{}\mathbf{D}\frac{d}{dt}i_{fd}\end{aligned} \tag{5.44}$$

After some manipulation and grouping like terms, the result can be expressed as:

$$\frac{d}{dt}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} = \left[\mathbf{L}_{\mathbf{mqd}}\check{}^{-1} + \mathbf{C}\right]^{-1}\left\{\frac{d}{dt}\begin{bmatrix}i_{qs}\\ i_{ds}\end{bmatrix} - \mathbf{A}\begin{bmatrix}y_q\\ y_d\end{bmatrix} - \mathbf{B}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} - \mathbf{D}\frac{d}{dt}i_{fd}\right\} \tag{5.45}$$

Since the matrix $\mathbf{L}_{\mathbf{mqd}}\check{}$ is symmetric and the matrix $\mathbf{C}$ added to it is a diagonal matrix, the inverse of the matrix $\left[\mathbf{L}_{\mathbf{mqd}}\check{}^{-1} + \mathbf{C}\right]$ is also symmetric and can be expressed as:

$$\mathbf{L}_{mqd} = \begin{bmatrix}L_{mqq} & L_{mdq}\\ L_{mdq} & L_{mdd}\end{bmatrix} \tag{5.46}$$

Thus, (5.45) becomes:

$$\frac{d}{dt}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} = \mathbf{L}_{mqd}\left\{\frac{d}{dt}\begin{bmatrix}i_{qs}\\ i_{ds}\end{bmatrix} - \mathbf{A}\begin{bmatrix}y_q\\ y_d\end{bmatrix} - \mathbf{B}\begin{bmatrix}\lambda_{mq}\\ \lambda_{md}\end{bmatrix} - \mathbf{D}\frac{d}{dt}i_{fd}\right\} \tag{5.47}$$

Equation (5.47) can now be substituted in the stator *qd* voltage equation (5.39) to eliminate the magnetising flux linkage derivative terms. After simplifying and grouping terms, the resulting expression of the stator *qd* voltage becomes:

$$\begin{aligned}\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} &= r_s \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \omega_r L_{ls} \begin{bmatrix} i_{ds} \\ -i_{qs} \end{bmatrix} + \left\{ \begin{bmatrix} L_{ls} & 0 \\ 0 & L_{ls} \end{bmatrix} + \mathbf{L}_{mqd} \right\} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} \\ &+ \left\{ \begin{bmatrix} 0 & \omega_r \\ -\omega_r & 0 \end{bmatrix} - \mathbf{L}_{mqd}\mathbf{B} \right\} \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} - \mathbf{L}_{mqd}\mathbf{A} \begin{bmatrix} y_q \\ y_d \end{bmatrix} - \mathbf{L}_{mqd}\mathbf{D}\frac{d}{dt} i_{fd}\end{aligned} \tag{5.48}$$

By applying the inverse transformation matrix $[\mathbf{K}_s(\theta_r)]^{-1}$ to (5.48), the *dq* stator voltages can be transformed to their corresponding *abc* phase variable equivalent. However, before this transformation is applied, the rotor internal state variables and their derivatives need to be computed.

Rotor State Variables

Adopting similar rotor network state variables partitions as shown in [190], the internal rotor state vectors y_q and y_d can be defined as follows:

$$[y_q] = \begin{bmatrix} y_{q1} \\ \mathbf{y_{qn}} \end{bmatrix}, [y_d] = \begin{bmatrix} y_{d1} \\ y_{d2} \\ \mathbf{y_{dm}} \end{bmatrix} \tag{5.49}$$

where y_{q1} and y_{d1} are the first elements of the vectors y_q and y_d and y_{d2} is the second element of vector y_d. These elements are separated from the remaining y_q & y_d vectors elements which are represented by $\mathbf{y_{qn}}$ and $\mathbf{y_{dm}}$ for convenience respectively.

Solving for the first element y_{q1} of state vector y_q by substituting the rotor *q*-axis current equation (5.17) into the stator *q*-axis current equation (5.37) and also using $i_{mq} = \lambda_{mq}/\check{L_{mq}}$ gives:

$$i_{qs} = \frac{\lambda_{mq}}{\check{L}_{mq}} + \begin{bmatrix} \frac{1}{L_{kq1}} & \frac{1}{L_{kq2}} & . \end{bmatrix} \left[\begin{bmatrix} y_{q1} \\ \mathbf{y_{qn}} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ . \end{bmatrix} \begin{bmatrix} \lambda_{mq} \end{bmatrix} \right] \tag{5.50}$$

Expressing in terms of y_{q1} gives the equation that allows the computation of the rotor network q-axis state variables:

$$y_{q1} = L_{kq1} i_{qs} - L_{kq1}\left(\frac{1}{\check{L}_{mq}} + \frac{1}{L_{kq1}} + \frac{1}{L_{kq2}} + .\right)\lambda_{mq} - L_{kq1}\left(\frac{y_{q2}}{L_{kq2}} + \frac{y_{q3}}{L_{kq3}} + .\right) \tag{5.51}$$

Substituting (5.51) into the expression of y_q in (5.49) gives the equation for computing the q-axis rotor internal state vector as:

$$[y_q] = \begin{bmatrix} L_{kq1} i_{qs} \\ 0_n \end{bmatrix} + \begin{bmatrix} \frac{-L_{kq1}}{L''_{mq}}\lambda_{mq} - L_{kq1}\left(\frac{y_{q2}}{L_{kq2}} + \frac{y_{q3}}{L_{kq3}} + .\right) \\ \mathbf{y_{qn}} \end{bmatrix} \tag{5.52}$$

where L''_{mq} is magnetising q-axis sub-transient inductance given by:

$$L''_{mq} = \left[\frac{1}{\check{L}_{mq}} + \frac{1}{L_{kq1}} + \frac{1}{L_{kq2}} + .\right]^{-1} \tag{5.53}$$

Carrying out a similar analysis on the d-axis rotor network state vector y_d by substituting the rotor d-axis current (5.9) into the stator d-axis current (5.37) and also using the field current (5.9) and simplifying gives:

$$\begin{bmatrix} y_{d1} \\ y_{d2} \end{bmatrix} = \begin{bmatrix} 0 & -L_{fd} \\ L_{kd1} & L_{kd1} \end{bmatrix} \begin{bmatrix} i_{ds} \\ i_{fd} \end{bmatrix} + \begin{bmatrix} 0 & -L_{fd} \\ L_{kd1} & L_{kd1} \end{bmatrix} \begin{bmatrix} (-\lambda_{md}\frac{1}{L''_{md}} - \frac{y_{d3}}{L_{kd_2}} - \frac{y_{d4}}{L_{kd_3}}.) \\ \frac{\lambda_{md}}{L_{fd}} \end{bmatrix} \tag{5.54}$$

where L''_{md} is magnetising d-axis sub-transient inductance given by:

$$L''_{md} = \left[\frac{1}{\check{L}_{md}} + \frac{1}{L_{fd}} + \frac{1}{L_{kd1}} + \frac{1}{L_{kd2}} + .\right]^{-1} \tag{5.55}$$

Similarly substituting (5.54) into the expression of y_d in (5.49) gives the equation for computing the d-axis rotor internal state vector as:

$$[y_d] = \begin{bmatrix} -L_{kd1} i_{fd} \\ L_{kd1}(i_{ds} + i_{fd}) \\ 0_m \end{bmatrix} + \begin{bmatrix} -\lambda_{md} \\ -L_{kd1}(\frac{\lambda_{md}}{L''_{md}} - \frac{\lambda_{md}}{L_{fd}} + \frac{y_{d3}}{L_{kd_2}} + \frac{y_{d4}}{L_{kd_3}} + .) \\ \mathbf{y_{dm}} \end{bmatrix} \tag{5.56}$$

It can be seen from equations (5.52) and equation (5.56) that y_q and y_d are only functions of the stator current inputs i_{qds} , field current i_{fd} and the state variables λ_{mqd} &y_{qdn}.

Equation (5.52) and (5.56) can be combined and expressed in matrix form similar to that of (5.48) to give:

$$\begin{bmatrix} y_q \\ y_d \end{bmatrix} = \mathbf{E} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \mathbf{F} i_{fd} + \mathbf{G}(\lambda_{mqd}, y_{qd}) \tag{5.57}$$

where the $\mathbf{E}, \mathbf{F}$ & $\mathbf{G}(\lambda_{qd}, y_{mqd})$ are block matrices given in Appendix A. The matrix $\mathbf{G}(\lambda_{qd}, y_{mqd})$ is a function of the qd magnetising flux linkage and rotor internal state vectors.

The equation (5.57) for the rotor internal state vectors derived above can now be substituted into the equation (5.48) for the qd stator voltages to give:

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = r_s \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \omega_r L_{ls} \begin{bmatrix} i_{ds} \\ -i_{qs} \end{bmatrix} + \begin{bmatrix} L_{ls} & 0 \\ 0 & L_{ls} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \mathbf{L}_{mqd} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} - \mathbf{L}_{mqd} \mathbf{AE} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix}$$
$$- \mathbf{L}_{mqd} \mathbf{AF} i_{fd} - \mathbf{L}_{mqd} \mathbf{D} \frac{d}{dt} i_{fd} \left\{ -\mathbf{L}_{mqd} \mathbf{AG}(\lambda_{mqd}, y_{qd}) + \begin{bmatrix} 0 & \omega_r \\ -\omega_r & 0 \end{bmatrix} \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} - \mathbf{L}_{mqd} \mathbf{B} \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} \right\} \tag{5.58}$$

The term in curly brackets in (5.58) above is a function of the magnetising flux linkages and the rotor internal state vectors and represents the qd sub-transient voltages. For simplicity, this term will be denoted by e''_{qds} henceforth.

Thus, the above equation becomes:

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = r_s \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \omega_r L_{ls} \begin{bmatrix} i_{ds} \\ -i_{qs} \end{bmatrix} + \begin{bmatrix} L_{ls} & 0 \\ 0 & L_{ls} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \mathbf{L}_{mqd} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} - \mathbf{L}_{mqd}\mathbf{AE} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} - \mathbf{L}_{mqd}\mathbf{AF} i_{fd} - \mathbf{L}_{mqd}\mathbf{D} \frac{d}{dt} i_{fd} + \begin{bmatrix} e''_{qs} \\ e''_{ds} \end{bmatrix} \tag{5.59}$$

Equation (5.59) can be transformed to physical variables i.e. stator phase voltages, stator inductance and resistance matrices that forms the stator subsystem of the VBR formulation.

Field Winding Voltage

To complete the formulation for the field winding, the magnetising flux linkage derivative term $\frac{d}{dt}\lambda_{md}$ and the rotor internal state vector y_d in the field voltage (5.11) are eliminated using (5.45) and (5.57) to yield:

$$v_{fd} = \left[\mathbf{HE}_d - \mathbf{L}_{\overline{mqd}}\mathbf{AE}\right] \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + (\mathbf{HF}_d - \mathbf{L}_{\overline{mqd}}\mathbf{AF}) i_{fd} + (L_f d - \mathbf{L}_{\overline{mqd}}\mathbf{D}) \frac{d}{dt} i_{fd} + \mathbf{L}_{\overline{mqd}} \frac{d}{dt} \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + \left\{ -\mathbf{B} \begin{bmatrix} \lambda_{mq} \\ \lambda_{md} \end{bmatrix} - \mathbf{L}_{\overline{mqd}}\mathbf{AG}(\lambda_{mqd}, y_{mqd}) + \mathbf{HG}(\lambda_{mqd}, y_{mqd})_d - \frac{r_{fd}}{L_{fd}} \lambda_{md} \right\} \tag{5.60}$$

where, the matrix $\mathbf{L}_{\overline{mqd}}$ denotes the second row of matrix $\mathbf{L}_{mqd}$ given by (5.46) and the matrices $\mathbf{E}_d$, $\mathbf{F}_d$ and $\mathbf{G}(\lambda_{mqd}, y_{mqd})_d$ are the respective bottom sub-matrices of the block matrices **E, F, G** given in appendix A.

Similar to (5.59) the term in curly brackets in above (5.60) is a function of the magnetising flux linkages and the rotor internal state vectors and represents a sub-transient component of the voltage. For simplicity, this term will be denoted by e''_{fd} henceforth. The field voltage becomes:

$$v_{fd} = \left[\mathbf{HE}_d - \mathbf{L}_{\overline{mqd}}\mathbf{AE}\right]\begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + (\mathbf{HF}_d - \mathbf{L}_{\overline{mqd}}\mathbf{AF})i_{fd}$$
$$+(L_f d - \mathbf{L}_{\overline{mqd}}\mathbf{D})\frac{d}{dt}i_{fd} + \mathbf{L}_{\overline{mqd}}\frac{d}{dt}\begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} + e''_{fd} \tag{5.61}$$

5.3.4 qd to abc $\cdots$ n Transformation

The derived *qd* stator voltages (5.59) and the field voltage (5.61) above can now be transformed from the *dq* reference frame to the $abc\cdots n$ physical reference frame. For clarity and easy implementation in simulation packages, (5.59) and (5.61) can be readily combined using block matrices to yield:

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = \begin{bmatrix} r_s\mathbf{I}_{[2\times2]} & 0_{[2\times1]} \\ 0_{[1\times2]} & \mathbf{HF}_{d_{[1\times1]}} \end{bmatrix}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \omega_r L_{ls}\begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \begin{bmatrix} L_{ls}\mathbf{I}_{[2\times2]} & 0_{[2\times1]} \\ 0_{[1\times2]} & L_{fd} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix}$$
$$+\begin{bmatrix} \mathbf{L}_{mqd_{[2\times2]}} & -\mathbf{L}_{mqd}\mathbf{D}_{[2\times1]} \\ \mathbf{L}_{\overline{mqd}_{[1\times2]}} & -\mathbf{L}_{\overline{mqd}}\mathbf{D}_{[1\times1]} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \begin{bmatrix} -\mathbf{L}_{mqd}\mathbf{AE}_{[2\times2]} & -\mathbf{L}_{mqd}\mathbf{AF}_{[2\times1]} \\ -\mathbf{L}_{\overline{mqd}}\mathbf{AE}_{[1\times2]} & -\mathbf{L}_{\overline{mqd}}\mathbf{AF}_{[1\times1]} \end{bmatrix}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \begin{bmatrix} e''_{qs} \\ e''_{ds} \\ e''_{fd} \end{bmatrix} \tag{5.62}$$

where $\mathbf{HE}_d$ in the field voltage equation simplified to zero.

For convenience, the matrices $\mathbf{R}_s, \mathbf{L}_s, \mathbf{R}_m$ & $\mathbf{L}_m$ will be adopted to represent the respective matrices of (5.62) above to give:

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ v_{fd} \end{bmatrix} = \mathbf{R}_s\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \omega_r L_{ls}\begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \mathbf{L}_s\frac{d}{dt}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix}$$
$$+\mathbf{R}_m\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \mathbf{L}_m\frac{d}{dt}\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{fd} \end{bmatrix} + \begin{bmatrix} e''_{qs} \\ e''_{ds} \\ e''_{fd} \end{bmatrix} \tag{5.63}$$

To account for the additional field voltage term in the inverse transformation, the transformation matrix given in (5.31) is modified as follows:

$$\begin{bmatrix} \mathbf{f}_{qd_s} \\ v_{fd} \end{bmatrix} = [\mathbf{K}_s(\theta_r)] \begin{bmatrix} \mathbf{f}_{abc..n_s} \\ f_{fd} \end{bmatrix} \tag{5.64}$$

where;

$$\mathbf{K}_s(\theta_r) = \begin{bmatrix} \check{\mathbf{K}}_s(\theta_r) & 0_{[2\times 1]} \\ 0_{[1\times N]} & 1 \end{bmatrix} \tag{5.65}$$

Applying (5.64) and (5.65) to (5.63) yields the corresponding transformed variables in $abc\cdots n$ reference frame as:

$$\begin{aligned} \begin{bmatrix} v_{abc\cdots n} \\ v_{fd} \end{bmatrix} = \mathbf{K}_s(\theta_r)^{-1}\mathbf{R}_s\mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} + \mathbf{K}_s(\theta_r)^{-1}(\omega_r L_{ls} \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix}) \\ + \mathbf{K}_s(\theta_r)^{-1}\mathbf{L}_s\frac{d}{dt}(\mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix}) + \mathbf{K}_s(\theta_r)^{-1}\mathbf{R}_m\mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} \\ + \mathbf{K}_s(\theta_r)^{-1}\mathbf{L}_m\frac{d}{dt}(\mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix}) + \mathbf{K}_s(\theta_r)^{-1} \begin{bmatrix} e''_{qs} \\ e''_{ds} \\ e''_{fd} \end{bmatrix} \end{aligned} \tag{5.66}$$

Using the attributes of the transformation matrix $\mathbf{K}_s(\theta_r)$ alluded to in (5.33) and (5.34), the above equation simplified to:

$$\begin{bmatrix} v_{abc\cdots n} \\ v_{fd} \end{bmatrix} = \mathbf{R}_s \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} + \mathbf{L}_s \frac{d}{dt} \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} + \mathbf{K}_s(\theta_r)^{-1} (\omega_r L_{ls} \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix})$$
$$+\omega_r \mathbf{K}_s(\theta_r)^{-1} \mathbf{L}_s \frac{d}{d\theta}(\mathbf{K}_s(\theta_r)) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} + \mathbf{K}_s(\theta_r)^{-1} \mathbf{R}_m \mathbf{K}_s(\theta_r) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix}$$
$$+\omega_r \mathbf{K}_s(\theta_r)^{-1} \mathbf{L}_m \frac{d}{d\theta}(\mathbf{K}_s(\theta_r)) \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} + \mathbf{K}_s(\theta_r)^{-1} \mathbf{L}_m \mathbf{K}_s(\theta_r) \frac{d}{dt} \begin{bmatrix} i_{abc\cdots n} \\ i_{fd} \end{bmatrix} + \mathbf{K}_s(\theta_r)^{-1} \begin{bmatrix} e''_{qs} \\ e''_{ds} \\ e''_{fd} \end{bmatrix} \tag{5.67}$$

This generic equation can be applied to machines with multiple number of stator phases and windings to give the VBR model stator variables of this formulation.In this work the standard equation has been modified to incorporate the multiphase machine topology presented in this thesis. The Park and Clarke transform matrices have been modified to enable multiphase transformations of the input and output VBR model variables between the physical *abc* domain and the *dq* domain and vice versa.

5.4 Model Implementation

The derived voltage behind reactance machine equations were implemented in **PLECS** simulation software that runs in Matlab/Simulink simulation software. The model implemented shown in figure 7.11 consist of: 24 stator phases, 2 q-axis damper windings, 1 field winding and one d-axis damper winding. The C-scripting feature of PLECS was used to implement the system equations directly in C programming language. The rotor speed and rotor position were computed by solving the machine mechanical subsystem equation;

$$J\frac{d}{dt}\omega_m + F\,\omega_m = T_e - T_m \tag{5.68}$$

where J is the inertia, F is the friction coefficient, T_m is the mechanical shaft torque and T_e is the electrical torque.

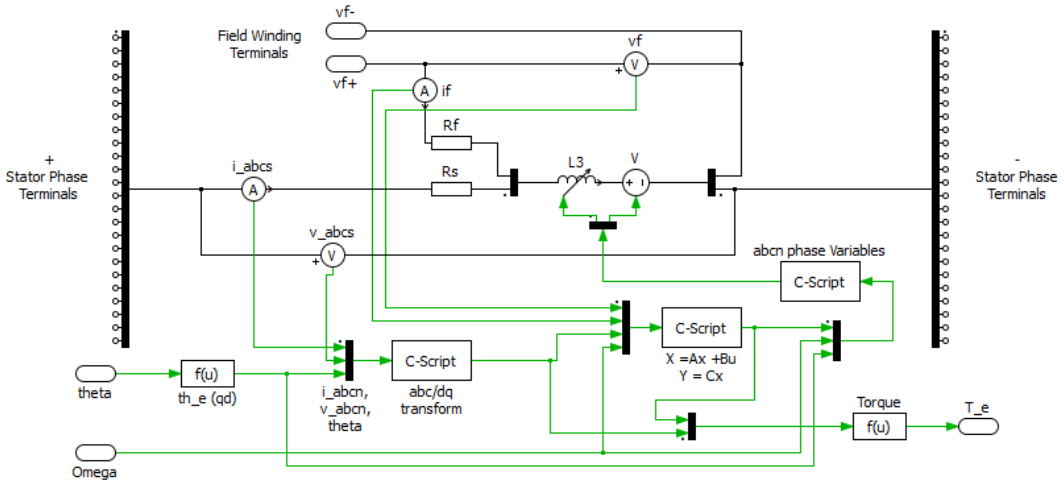

Fig. 5.3 Machine Simulation Model Implementation in PLECS

A similar model was also implemented for the analysis of machine topology with an odd number of stator phases. In this case a 15 phase machine model was implemented in PLECS using the same approach to that used for the even numbered 24 phase machine. The developed models were also instrumental in the topology comparative analysis between even and odd number topologies presented in chapter 3.

5.4.1 Model Limitations

The equations derived for the VBR machine model implementation discussed so far assumed sinusoidal machine airgap flux and also does not account for the armature reaction effects. As alluded to earlier, both the trapezoidal airgap flux and armature reaction have an impact on the operational characteristics of the multiphase electronically commutated dc machines. To account for these features some simplifying assumptions were made in the model implementation to account for these effects. Further work will be required to accurately model these two effects in the machine simulation models.

Machine Trapezoidal Airgap Flux

The dq Park transformations used in the machine variables transformation are strictly valid for sinusoidally varying ac variables. Owing to the non-sinusoidal phase currents and trapezoidal back emfs of this machine topology, accurate dq reference frame transformations of the currents & voltages cannot be easily accomplished. As such, simplifying assumptions have been made to treat the variables as sinusoidal quantities

in the transformations although they are in fact trapezoidal. This assumption is not unreasonable, considering the dominant fundamental components are still sinusoidal.

Machine Armature Reaction

Typical mechanically brush commutated DC machine benefit from commutator poles which act to counter the undesirable effects of armature reaction. Armature reaction which is dependent on the magnitude of machine stator current, creates a triangular airgap flux distribution which act to distort the trapezoidal airgap flux distribution [35]. This means the induced machine back emfs are no longer trapezoidal. Figure 5.4 and figure 5.5 shows the effect of armature reaction on the machine phase voltages when operating in motoring or generating modes. Armature reaction has little impact on the machine torque as the rms value of the flux will remain the same despite the distortion if no saturation occurs. Its however likely to have a noticeable impact on machine saturation characteristics since it causes an uneven flux distribution in the machine.

No attempt to model machine saturation effects was included in the developed models. As such, armature reaction was considered to have no effect on the machine torque production. Instead, experimental results showed that it has a more noticeable impact on the machine phase voltage available to support electronic commutator phase current commutation.

To account for the trapezoidal back emf voltages and the armature reaction effects in the models, the calculated back emfs from the VBR models were modified to account for the additional harmonics present in the resultant waveforms. Fast Fourier Transforms of the measured machine voltage waveforms were used to obtain the dominant harmonics of the resultant voltages due to trapezoidal airgap flux and armature reaction effects. The VBR model voltages E_{ph} were modified by a generic fourier expression;

$$E_{ph} = e''_{vbr} \sum_{n=1,3,5,\ldots}^{19} (\hat{a}\cos(n\theta + \phi_n)) \tag{5.69}$$

where, e''_{vbr} is the computed VBR voltage amplitude, θ is the phase angle, $\hat{a}$ is the per unit peak amplitude of the harmonic, n is the harmonic order and ϕ_n is the harmonic phase angle. It was observed that including odd harmonics up to the 19th harmonic gave good results. Figure 5.6 and figure 5.7 show the simulated machine waveforms

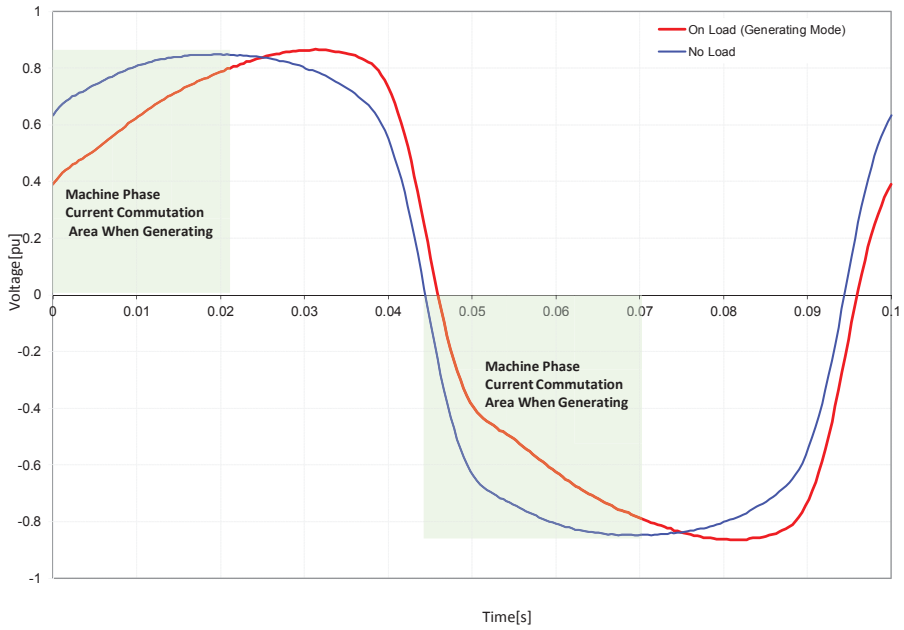

Fig. 5.4 Effect of Armature Reaction of Machine Back emf in Generating Mode

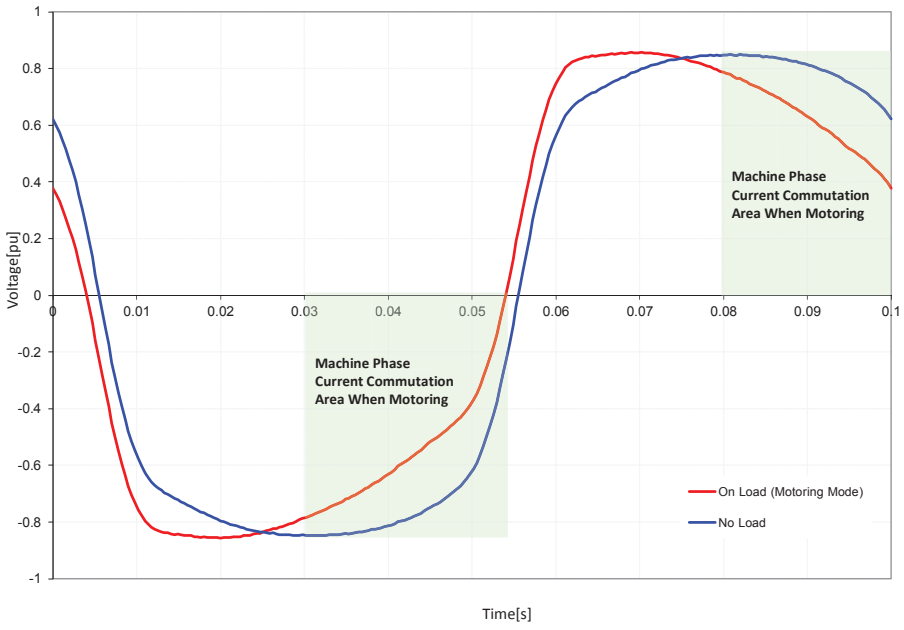

Fig. 5.5 Effect of Armature Reaction of Machine Back emf in Motoring Mode

and FFT plots for a 15 phase and 24 phase machine topologies when fed from ideal dc link current source. The modification above gave a good results when phase current commutations occurred close to the q-axis. It however did not account for the sagging

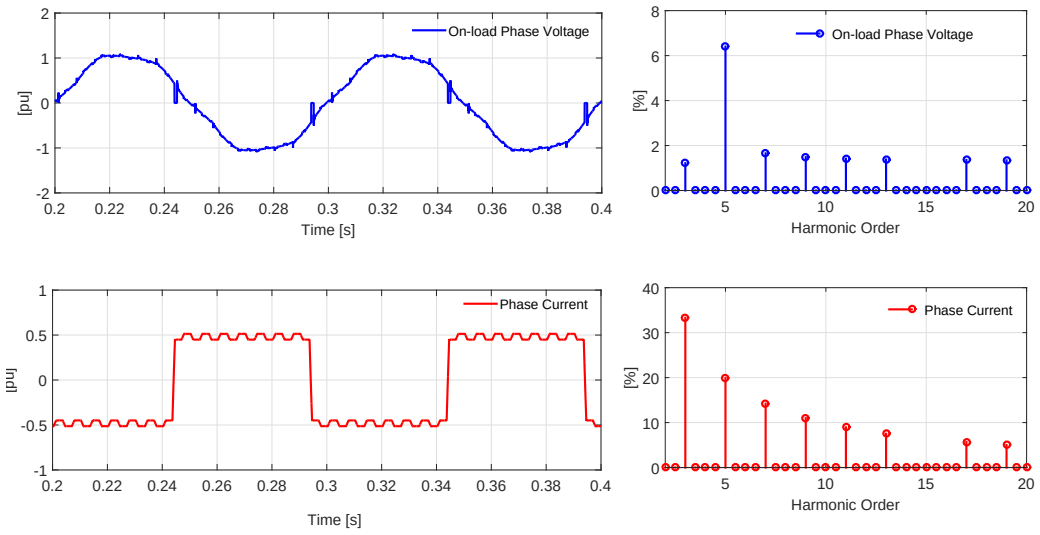

Fig. 5.6 Simulated 15 Phase Machine with Trapezoidal Voltage Waveforms and Armature Reaction

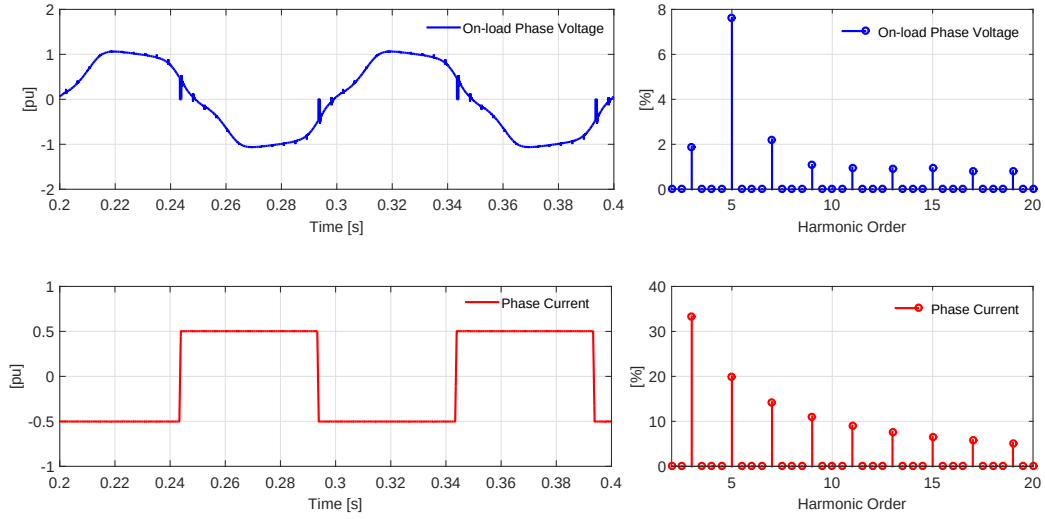

Fig. 5.7 Simulated 24 Phase Machine with Trapezoidal Voltage Waveforms and Armature Reaction

in phase voltage that results when phase current commutation events are not close to the q-axis as depicted in figure 5.8.

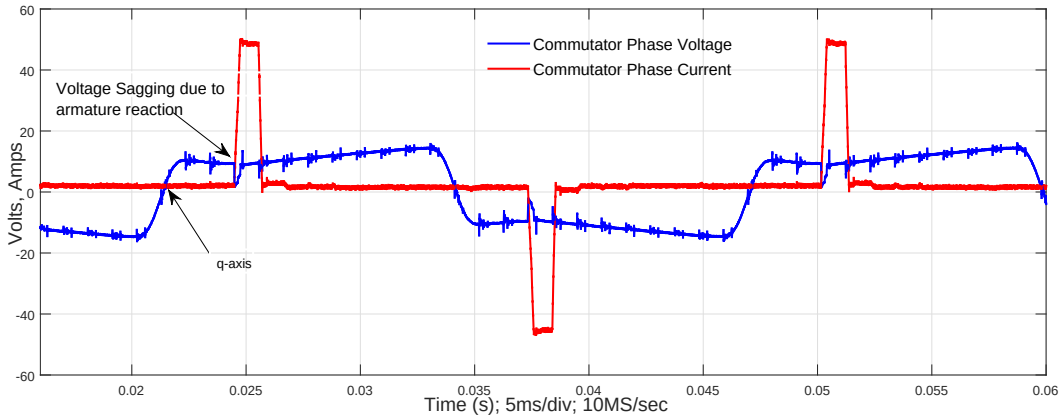

Fig. 5.8 Experimental Measurement of Armature Reaction Effects on Phase Commutation Voltage

5.5 Summary

The equations governing the VBR machine model formulation for multiphase electronically commutated DC machines has been presented. The model was implemented in PLECS for machines with 15 and 24 stator phases. No artificial numerical snubber circuits were included when the machine model was interfaced to the rest of the power electronic converter system. Simulation results confirmed that power electronic converters can be easily interfaced to the machine model without compromising the stability of the simulations and without noticeable degradation in simulation time. The generic formulation of this model presented here makes it applicable to various machine converter topologies for detailed studies and characterisation of these drive systems. Further refinements will be required to accurately model the trapezoidal back emf and armature reaction effects. An attempt has been made in the developed model to account for these effects but further refinements will be required to improve the accuracy.

Chapter 6

Control Design

6.1 Introduction

Before discussing the overall control schemes proposed and implemented for the machine and converter topologies considered in this work, the formulation and implementation of the controller type used for regulation of the control variables is described in detail here. The control loops implemented in this work are based on an elegant pole placement method that uses the polynomial solution of the Diophantine equation [201], [202], [203] . The controller pole placement design aims to find a controller that yields a closed loop system with a specified characteristic polynomial. The main goal is to get a controller design that gives good reference signal tracking characteristics. An additional goal is also to have a controller that gives good plant disturbance rejection performance. This controller design is based on defining three polynomials (R, S and T) to yield a closed loop system with the desired performance characteristics. The main attractions of this polynomial controller formulation is that it can selectively & independently manage the dynamic reference signal tracking and disturbance signal rejection dynamics whilst at the same time accounting for the sampling time delays inherent in digital control systems. In the formulation presented in this work, the desired controller tuning parameters such as required damping (ζ) and bandwidth (ω) are incorporated as inputs in the controller polynomials structure to facilitate easy controller tuning. This chapter describes the controller design approach adopted,

first in the *s*-domain then in the *z*-domain to expose the inherent sampling delays compensation attributes for practical digital controller implementation.

6.2 Polynomial RST Controller Design

This section outlines the design of the polynomial controller, referred to as **RST** controller. The generic controller design formulated here forms the basis of all the major control loops employed in the machine control strategy discussed in later chapters and experimental and simulation results presented in this work. For completeness, a generic controller structure will be presented. However, since the main controlled subsystems for the machine and converter drive topology presented in this work such as; machine flux control, current control and speed control are first order systems, the design outlined here will be limited to first order systems.

6.2.1 Controller Structure

The RST control structure consists of three polynomial terms **R,S & T**, hence its name. The degree or order of the polynomials and the structure of the controller are formulated such that the desired controller performance parameters such as system damping, control bandwidth, anti-saturation characteristics and feedback sampling delay compensation attributes are inherent in the formulation.

The formulation presented here introduces two degrees of freedom in the controller structure, i.e. (a) disturbance rejection characteristics and (b) reference signal tracking performance. The R and S polynomial filters facilitate disturbance signal rejection to guarantee the desired regulation performance and the T polynomial filter facilitates the desired reference signal tracking performance [201]. With this polynomial controller structure, the R-S-T polynomials are generic polynomials that can be chosen such that any controller type e.g. Proportional plus Integral (PI), Integral plus Proportional (IP), Proportional plus Integral plus Derivative (PID) controllers can be synthesised by proper selection of the R, S & T polynomials. This controller formulation enables different levels of disturbance rejection and signal tracking performance to be achieved.

For a given system, the system response is mainly characterised by its poles. With the knowledge of these system poles, robust pole placement (assignment) method is exploited in the RST controller design to specify the desired closed loop system response (plant & controller). Figure 6.1 below shows a schematic of an RST controller and the controlled system (plant) with plant disturbance (plant noise). A generic design approach is adopted in this chapter.

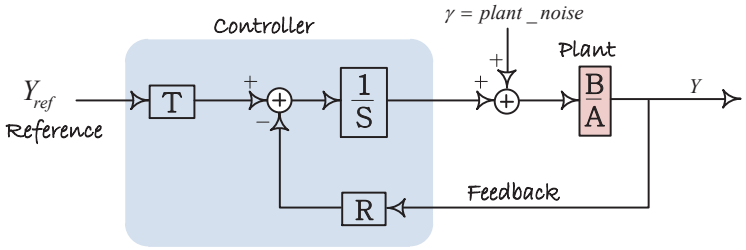

Fig. 6.1 R-S-T Controller Structure

6.2.2 Design Method Adopted

Owing to the generic nature of the RST control formulation, it is applicable to plant models of any order, featuring stable and unstable zeros. The choice of the degree or order of the RST polynomials presents an additional degree of freedom in the overall controller formulation which can yield some beneficial characteristics on the final discretized digital controller implementation [204]. For practical implementation of the controller for this work, two choices are possible for the selection of the order or degrees of the controller polynomials. The only assumption for both cases is that polynomials **A(s)** and **B(s)** characterising the plant have no common factors, where **B(s)** denotes the numerator polynomial and **A(s)** the denominator polynomial respectively.

The R, S & T controller polynomials have the generic form given by:

$$R(s) = r_0 + r_1 s + r_2 s^2 + \cdots + r_n s^{n_r} \tag{6.1}$$

$$S(s) = s_0 + s_1 s + s_2 s^2 + \cdots + s_n s^{n_s} \tag{6.2}$$

$$T(s) = t_0 + t_1 s + t_2 s^2 + \cdots + t_n s^{n_t} \tag{6.3}$$

where the subscripted *r, s, t* terms in the above denote the polynomial coefficients, and n_r, n_s, n_t denote the n^{th} order or degree of the respective polynomial.

The two design options are given below as;

Option 1:

In this first option, the orders or degrees of the control polynomials are based on the following constraints, where $\Lambda(S)$ denotes the order or degree of the S polynomial;

$$\Lambda(S) = \Lambda(R) = \Lambda(A) \tag{6.4}$$

and

$$\Lambda(D) = 2\Lambda(A) \tag{6.5}$$

where **D** is the polynomial of the closed loop system characteristic equation defined as:

$$D = AS + BR \tag{6.6}$$

Option 2:

In this second option, the orders or the control polynomials are based on the following constraints;

$$\Lambda(S) = \Lambda(A) + 1 \tag{6.7}$$

$$\Lambda(R) = \Lambda(A) \tag{6.8}$$

$$\Lambda(D) = 2\Lambda(A) + 1 \tag{6.9}$$

where D is defined by (6.6).

Provided the digital control system sampling frequency is sufficiently high, the effect of sampling delays can be negligible. However, high digital control sampling frequencies come at the expense of additional cost and increased potential of instability

due to additional phase shift introduced by the delays [205–207] . As such in cost sensitive applications minimising the impact of sampling delays can be an attractive cost effective option. In general, the effects of delays in closed-loop feedback systems resemble the effects of lowering the sampling frequency. Physically, this makes sense as the controller is forced to make use of old information (information about the output at some time in the past, rather than in the present) in determining the output it supplies to the plant.

Analysis of the above two options revealed that both options give similar performance in the *s*-domain. However, in the *z*-domain, the second option was found to yield superior performance. This is attributed to the fact that this option accounts for the digital controller sampling delays incurred in signal sampling on real practical digital controllers. This feature will be highlighted in the discrete formulation discussion later in this chapter.

6.3 s - Domain Controller Design

As alluded to earlier, the controller design described here will be limited to first order system. However, the same design process can be extended to higher order systems. A generalised first order system (plant) can be expressed in transfer function form as;

$$\frac{B(s)}{A(s)} = \frac{k}{s + a_0} \tag{6.10}$$

where the subscript s denotes s - domain, k is the open loop system gain and a_0 is the open loop system pole. The plant denominator polynomial A(s) is monic, i.e. it is normalised such that the coefficient of the term with highest power of s is one.

Applying the design constraints of option 2 in choosing the controller polynomials for this first order system results in the R polynomial being 1^{st} order and implies that the S polynomial is 2^{nd} order. The R and S polynomials can be expressed in generic form as:

$$R(s) = r_1 s + r_0 \tag{6.11}$$

$$S(s) = s_2 s^2 + s_1 s \tag{6.12}$$

For zero steady state error to obtain, the S polynomial must be of type one system, i.e. it must have at least one pole at the origin of the s plane. In other words, there must be a pure integrator in the forward loop of the system to ensure zero steady state error, this implies $s_0 = 0$, hence its omission in the formulation of (6.12).

6.3.1 Desired Dynamic Performance

Pole placement method has been chosen for the controller design owing to its versatility, i.e. it can be used for plant models of any order and for both design options highlighted above. With reference to Figure 6.1, the overall system close loop transfer function can be derived to give an output Y as:

$$Y(s) = \frac{T(s)B(s)}{A(s)S(s) + B(s)R(s)} Y_{ref} + \frac{B(s)S(s)}{A(s)S(s) + B(s)R(s)} \gamma \tag{6.13}$$

where Y_{ref} is the control reference, and γ is the plant disturbance (noise) and Y is the plant output. The dynamic response of the closed loop system is thus given by the characteristic equation G(s) which defines the desired closed loop poles of the system as:

$$G(s) = A(s)S(s) + B(s)R(s) = (s + a_0)(s_2 s^2 + s_1 s) + k(r_1 s + r_0) \tag{6.14}$$

Since the objective is to have a controller with the desired damping ratio ζ and desired bandwidths for both disturbance rejection (T_f^{-1}) and signal tracking (T_c^{-1}), two polynomials F(s) and C(s) with the desired system damping and bandwidths variables can be defined such that their product equation equals that of the system characteristic equation G(s). Formulating these in a generic sense yields:

$$F(s) = s_2 + 2\zeta \frac{1}{T_f} s + \frac{1}{T_f^2} \tag{6.15}$$

$$C(s) = s + \frac{1}{T_c} \tag{6.16}$$

where F(s) contains the desired dominant poles of the closed loop system and C(s) contains the auxiliary poles for robustness. Analysis has shown that good performance is achieved if the poles of C(s) are chosen to be three to five times faster than those of F(s), bearing in mind that the system response is dominated by the poles nearest to zero on the real axis of the s plane. The desired closed loop system poles are therefore placed by choosing the desired values of ζ, T_f and T_c to give the desired closed loop response.

6.3.2 R and S Polynomial Coefficients

The coefficients of the R and S polynomials can be readily computed by solving the Diophantine equation generated by equating the characteristic equation of the system G(s) to that of the desired target closed loop system i.e. product of F(s) & C(s) polynomials. A necessary condition for a unique solution to exists is that the order or degree of the desired closed loop polynomial must be the same as that of the closed loop characteristic equation, i.e. $\Lambda\{A(s)S(s) + B(s)R(s)\} = \Lambda\{F(s)C(s)\}$.

Thus,

$$A(s)S(s) + B(s)R(s) = F(s)C(s) \tag{6.17}$$

Using (6.10) and substituting (6.11), (6.12) and (6.15) into (6.17) gives;

$$(s+a_0)(s_2s^2 + s_1s) + k(r_1s + r_0) = (s_2 + 2\zeta\frac{1}{T_f}s + \frac{1}{T_f^2})(s + \frac{1}{T_c}) \tag{6.18}$$

Expanding and equating coefficients of the same order on both sides and expressing in matrix form gives;

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ a_0 & 1 & 0 & 0 \\ 0 & a_0 & k & 0 \\ 0 & 0 & 0 & k \end{bmatrix} \begin{bmatrix} s_2 \\ s_1 \\ r_1 \\ r_0 \end{bmatrix} = \begin{bmatrix} 1 \\ (2\frac{\zeta}{T_f} + \frac{1}{T_c}) \\ (\frac{1}{T_f^2} + 2\frac{\zeta}{T_f T_c}) \\ \frac{1}{T_f^2 T_c} \end{bmatrix} \tag{6.19}$$

Equation (6.19) can be simple expressed as;

$$S_{ylv}.\lambda_{\hbar} = \rho \tag{6.20}$$

where S_{ylv} is the Sylvester matrix from applied mathematics [208],[209] ,[210] whose coefficients are the plant system poles and zeros, $\lambda_{\hbar}$ is the matrix of the unknown S & R polynomial coefficients, ρ is the matrix whose elements are the desired characteristic equation polynomial coefficients.

The solution of (6.20) for the unknown coefficients of $\lambda_{\hbar}$ i.e. (s_2, s_1, r_1, r_0) can be solved by Gaussian elimination and is given by:

$$\lambda_{\hbar} = S_{ylv}^{-1}.\rho \tag{6.21}$$

6.3.3 T Polynomial Coefficients

The polynomial T has been chosen to impose a unit gain between input Y_{ref} and output Y in steady state in addition to the compensation of regulation dynamics. This can be accomplished by formulating the T polynomial such that:

$$T(s) = hF(s) \tag{6.22}$$

where h is a constant gain and F(s) is defined by (6.15)

Substituting (6.22) in the closed loop system transfer function (6.13) and simplifying gives:

$$Y(s) = \frac{hF(s)B(s)}{A(s)S(s) + B(s)R(s)} Y_{ref} + \frac{B(s)S(s)}{A(s)S(s) + B(s)R(s)} \gamma \tag{6.23}$$

For the system output Y(s) to follow the input in steady state i.e. *(s=0)* with a gain of one, the final value theorem can be applied to yield:

$$\frac{hF(0)B(0)}{A(0)S(0)+B(0)R(0)} = 1 \tag{6.24}$$

From (6.12) its clear that $S(0) = 0$, solving (6.24) gives the solution for the controller input gain h as;

$$h = \frac{R(0)}{F(0)} \tag{6.25}$$

6.3.4 Reference Signal Tracking and Noise Rejection

The RST controller formulation allows for the signal tracking and disturbance rejection performance to be selectively influenced. To enable this extra degree of freedom to be realised, (6.17) can be substituted in (6.23) to eliminate the terms $A(s)S(s)+B(s)R(s)$ in the denominator to yield:

$$Y(s) = \frac{hF(s)B(s)}{F(s)C(s)}Y_{ref} + \frac{B(s)S(s)}{F(s)C(s)}\gamma \tag{6.26}$$

which simplifies to;

$$Y(s) = \frac{hB(s)}{C(s)}Y_{ref} + \frac{B(s)S(s)}{F(s)C(s)}\gamma \tag{6.27}$$

Examination of (6.27) reveals that reference signal tracking dynamics are governed by the auxiliary poles of C(s) and the disturbance/noise rejection dynamics are governed by the dominant poles of F(s). Thus, there are two degrees of freedom that enable independent tuning of the controller for reference signal tracking and disturbance/noise rejection. This is a key desirable attribute of formulating the controller in this manner.

6.3.5 s - Domain Controller Implementation

For detailed studies of the dynamic behaviour of the drive system, its normal and convenient for the subsystems and the entire system to be modelled and analysed in the *s*-domain. For the controller derived above to be realised, the degree or order of all the numerator polynomials of the controller must be lower than those of the denominator polynomials. By manipulating (6.23) and dividing the all the R, S & T controller polynomials by F(s), the controller structure can be reformulated as shown in figure 6.2.

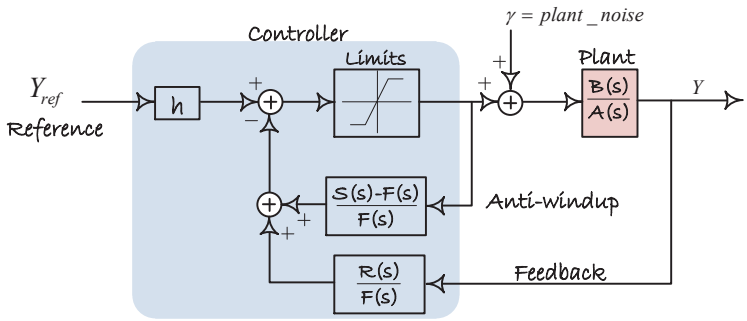

Fig. 6.2 Continuous Domain Controller Structure

Analysis of the transfer function of figure 6.1 and figure 6.2 shows that they are infact the same. However, formulating the structure as depicted in figure 6.2 brings with it an additional attractive benefit. As can be seen in this figure, It has an inherent saturation anti-windup feedback loop that ensures good dynamic performance particularly when the controller is operating in limit conditions. In the *s* domain studies, the computed controller polynomials can be used directly as depicted in this new controller structure.

6.4 z - Domain Controller Design

For practical realisation and implementation of the controller described on the experimental prototype drives for this work, the continuous *s*-domain controller derived above has to be discretized. A similar analysis to that carried out for the continuous *s*-domain controller design can be applied to the discretized plant and controller subsystems. The following sections briefly describe the *z*-domain design formulation for this controller.

6.4.1 Discrete Plant

As alluded to earlier, the controller design applied to this work focuses on first order systems, as such this section will be limited to first order systems. However, the design method employed can be readily extended to higher order systems. A generic first order plant can be described by (6.28), where *B(z)* and *A(z)* represent the discretized numerator and denominator polynomials of the plant respectively.

$$\frac{B(z)}{A(z)} = \frac{k_0}{z - z_a} \tag{6.28}$$

where $z_a = e^{-a_0 T_s}$, T_s is the controller sampling interval and k_0 is the discrete plant open loop gain.

From the above equation, for the plant to have the same steady state gain in the z-domain as in the s-domain, applying the final value theorem by substituting $z=1$ (similar to $s=0$ in the s-domain) to (6.28) using (6.10) gives;

$$\frac{k}{a_0} = \frac{k_0}{1 - z_a} \tag{6.29}$$

Using (6.29) to eliminate k_0 in (6.28) gives the expression of the discretized plant as;

$$\frac{B(z)}{A(z)} = \frac{\frac{k}{a_0}(1 - z_a)}{z - z_a} \tag{6.30}$$

6.4.2 Discrete R and S Controller Polynomials

The discretized R and S controller polynomials for the first order controller can be expressed in generic form with unknown polynomial coefficients as;

$$R(z) = r_1 z + r_0 \tag{6.31}$$

$$S(z) = s_2 z^2 + s_1 z - (s_2 + s_1) \tag{6.32}$$

where r_1, r_0, s_2, s_1 are the unknown R(z) and S(z) polynomial coefficients respectively. Note expressing the zero order term of (6.32) as shown guarantees a zero steady state error i.e. $S(z = 1) = 0$.

6.4.3 Desired Dynamic Performance

The equations that govern the signal tracking and disturbance rejection controller dynamic performance (6.15) and (6.16) will be recalled and expressed as follows for convenience of the ensuing formulation.

$$F(s) = s^2 + 2\zeta\omega s + \omega^2 \tag{6.33}$$

$$C(s) = (s + \omega_0) \tag{6.34}$$

where, ω_0 and ω are the signal tracking and disturbance rejection bandwidths set by the parameters T_c and T_f respectively and ζ is the desired closed loop system damping ratio.

The discrete signal tracking polynomial C(z) can be expressed in generic form as;

$$C(z) = (z + z_0) \tag{6.35}$$

where $z_0 = e^{-\omega_0 T_s}$.

From equation (6.33), the two roots of F(s) are $-\zeta\omega \pm j\omega\sqrt{1-\zeta^2}$. Thus, the discrete disturbance rejection polynomial F(z) can be expressed in generic form as;

$$F(z) = (z - z_1)(z - z_2) \tag{6.36}$$

where;

$$z_{1,2} = e^{-\omega T_s(\zeta \mp j\sqrt{1-\zeta^2})} \tag{6.37}$$

Expanding (6.36) using (6.37) yields;

$$F(z) = z^2 - 2\alpha\beta z + \alpha^2 \tag{6.38}$$

where $\alpha = e^{-\zeta\omega T_s}$ and $\beta = cos(\omega T_s\sqrt{1-\zeta^2})$.

Using equations (6.35) and (6.38), the discretized characteristic equation of the desired closed loop system can be written as;

$$F(z)C(z) = (z^2 - 2\alpha\beta z + \alpha^2)(z + z_0) \tag{6.39}$$

Similar to the *s*-domain analysis that gave (6.15), the discretized closed loop system (plant & controller) characteristic equation can be expressed using (6.30), (6.31) and (6.32) as;

$$A(z)S(z)+B(z)R(z)=(z-z_a)(s_2z^2+s_1z-s_2-s_1)+\frac{k}{a_0}(1-z_a)(r_1z+r_0) \quad (6.40)$$

6.4.4 R and S Polynomial Coefficients

The unknown polynomial coefficients of R(z) and S(z) are determined by solving the Diophantine equation generated by equating the closed loop system characteristic equation (6.40) to the desired closed loop system characteristic equation (6.39). Again as in the *s*-domain, the polynomial order of the two characteristic equations must be the same for a unique solution to exist i.e. $\Lambda(A(z)S(z)+B(z)R(z))=\Lambda(F(z)C(z))$.

Expanding the Diophantine equation and equating like powers coefficients on both sides and expressing the result in matrix form gives;

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ -z_a & 1 & 0 & 0 \\ -1 & -(1-z_a) & \frac{k}{a_0}(1-z_a) & 0 \\ z_a & z_a & 0 & \frac{k}{a_0}(1-z_a) \end{bmatrix} \begin{bmatrix} s_2 \\ s_1 \\ r_1 \\ r_0 \end{bmatrix} = \begin{bmatrix} 1 \\ -(2\alpha\beta+z_0) \\ \alpha^2+2\alpha\beta z_0 \\ -\alpha^2 z_0 \end{bmatrix} \quad (6.41)$$

The solution for the unknown coefficients of the discretized R(z) and S(z) polynomials in (6.41) can now be obtained by multiplying the resultant inverse of the Sylvester matrix with the matrix of the desired closed loop system coefficients similar to (6.20) and (6.21) of the *s*-domain.

6.4.5 T Polynomial Coefficients

Similar to the *s*-domain analysis, the polynomial T(z) is chosen to impose an input to output gain of unit in addition to facilitating controller regulation dynamics. Defining T(z) using a constant gain h_z such that;

$$T(z)=h_zF(z) \quad (6.42)$$

and substituting (6.42) in the equation that describe the closed loop system gives the system output gives;

$$Y(z) = \frac{h_z F(z)B(z)}{A(z)S(z)+B(z)R(z)}Y_{ref} + \frac{B(z)S(z)}{A(z)S(z)+B(z)R(z)}\gamma \tag{6.43}$$

Applying the final value theorem, for unit gain to obtain in steady state conditions implies:

$$Y(z=1) = \frac{h_z F(1)B(1)}{A(1)S(1)+B(1)R(1)} = 1 \tag{6.44}$$

Bearing in mind that S(1) = 0 for a zero steady state error to be guaranteed, (6.44) simplifies further to give the solution of the unknown T(z) polynomial gain h_z as;

$$h_z = \frac{R(1)}{F(1)} \tag{6.45}$$

6.4.6 z - Domain Controller Implementation

For practical realisation of the designed controller in a digital controller, the discretized controller polynomials can be readily expressed in ascending power of z^{-1}. Where z^{-1} is a delay function symbolizing the discrete controller's last sampled value.

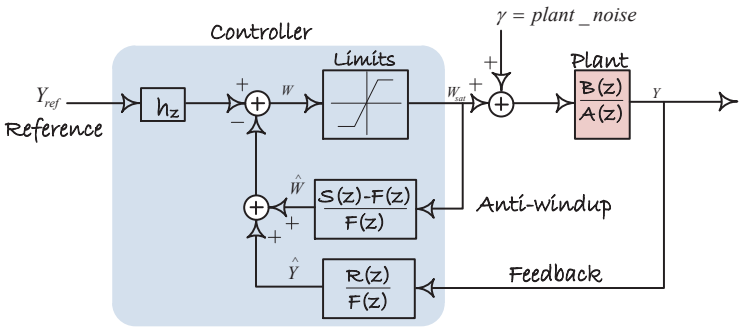

Fig. 6.3 Discrete Controller Structure

The discrete controller structure formulation alluded to in figure 6.2 is adopted by dividing the controller polynomials by F(z) and rearranging the resultant expression to give figure 6.3 with the controller equations:

$$\frac{S(z)-F(z)}{F(z)} = \frac{(\frac{s_1}{s_2}+2\alpha\beta)-(\frac{s_1+s_2}{s_2}-\alpha^2)z^{-1}}{1-2\alpha\beta z^{-1}+\alpha^2 z^{-2}}.z^{-1} \tag{6.46}$$

$$\frac{R(z)}{F(z)} = \frac{(r_1+r_0 z^{-1})}{1-2\alpha\beta z^{-1}+\alpha^2 z^{-2}}.z^{-1} \tag{6.47}$$

$$h_z = \frac{r_1+r_0}{1-2\alpha\beta+\alpha^{-2}} \tag{6.48}$$

Implementation in Control Hardware

The above equations can be normalized and readily expressed as difference equations for direct translation into any programming language such as C language for porting into digital control hardware.

The mathematical analysis above shows that (6.46) and (6.47) have extra multiplier terms with z^{-1} which inherently account for the feedback signals sampling delays encountered in practical digital controllers. This is attributed to the choice of controller polynomials highlighted earlier in 6.2.2. Analysis of the discretized form of option 1 of controller polynomials does not yield a discrete controller that inherently accounts for this controller sampling delay. Figure 6.4 shows simulated comparison of two options for the choice of the controller polynomials, for a first order system with a low controller sampling frequency of 100Hz. The top plot shows the controller reference signal, the $s-$domain controller response of option 2 and the $z-$domain controller response of both option 1 and option 2 for the same controller bandwidths and damping ratios. The bottom plot shows the controller output commands for the $s-$domain and $z-$ domain controller output commands for option 1 & 2. Its clear that option 2 gives better performance compared to option 1 for reduced controller sampling frequency.

The equations (6.31), (6.32) and (6.38) can be expressed in generic form with the polynomial coefficients $r_1, r_0, s_1, s_0, f_1, f_0$ where *F(z)* and *S(z)* are monic to give;

$$R(z) = r_1 z + r_0 \tag{6.49}$$

$$S(z) = z^2 + s_1 z + s_0 \tag{6.50}$$

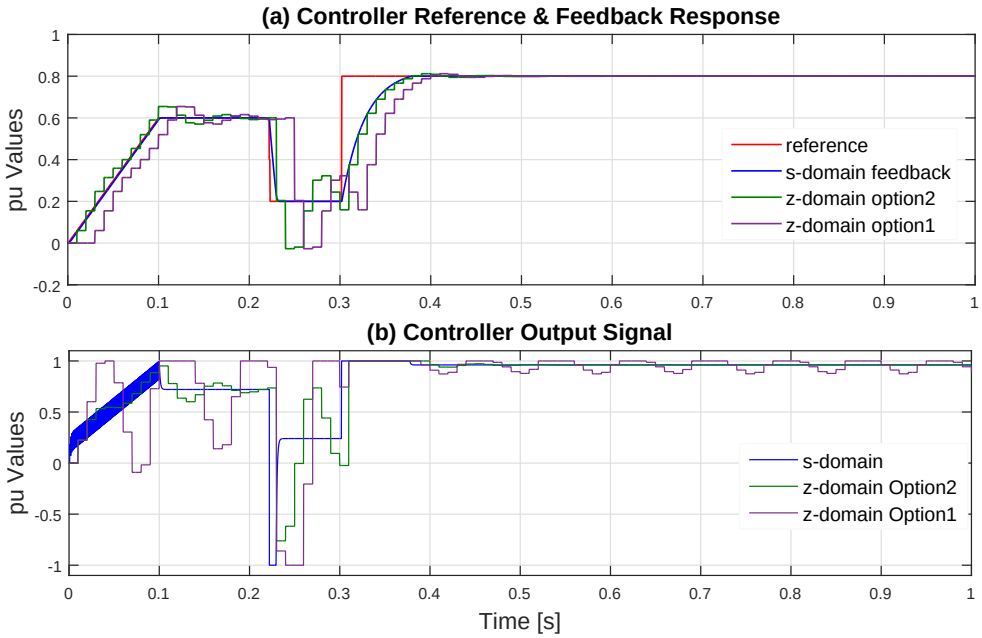

Fig. 6.4 Simulation of Controller Response for Controller Polynomial Order Option 1 & 2 for Low Controller Sampling Frequency.

$$F(z) = z^2 + f_1 z + f_0 \tag{6.51}$$

With reference to figure 6.3, the discrete controller algorithm can be implemented in control hardware as;

$$\hat{Y}_{(n)} = r_1 Y_{(n-1)} + r_0 Y_{(n-2)} - f_1 \hat{Y}_{(n-1)} - f_0 \hat{Y}_{(n-2)} \tag{6.52}$$

$$\hat{W}_{(n)} = (s_1 - f_1) W_{sat_{(n-1)}} + (s_0 - f_0) W_{sat_{(n-2)}} - f_1 \hat{W}_{(n-1)} - f_0 \hat{W}_{(n-2)} \tag{6.53}$$

$$W_{(n)} = h_z Y_{ref_{(n)}} - \hat{Y}_{(n)} - \hat{W}_{(n)} \tag{6.54}$$

The above equations can be easily and efficiently implemented in a digital controller. Figure 6.5 shows simulation of the controller closed loop dynamic behavior regarding reference signal tracking and plant noise disturbance rejection performance for step changes in plant disturbance.

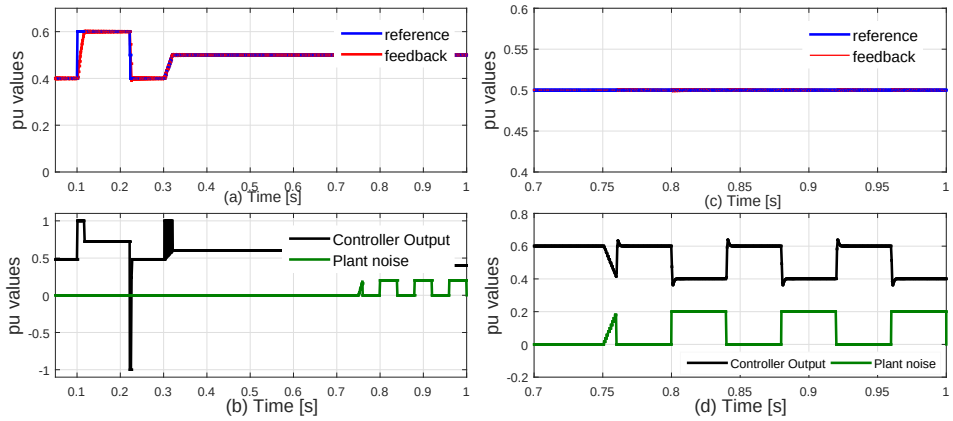

Fig. 6.5 Simulation Results of Closed-Loop Behaviour of Controller; (a) Reference and Feedback Signals, (b) Controller Output Signal and Plant Noise Disturbance, (c) Zoom of (a) Showing Noise Rejection, (d) Zoom of (b) Showing Noise Rejection Controller Response.

6.5 Summary

This chapter has presented the formulation and analysis of the controller design used as basis for all the major control loops implemented in the proposed control scheme for the converter and Machine topology considered in this work. The controller formulation and analysis has exposed the control parameters that enable independent control of dynamic reference signal tracking and plant noise disturbance rejection. It has also been shown in the analysis of the discrete implementation that careful selection of controller polynomial order can yield controllers that inherently accounts for the sampling delays incurred in real digital controller. The controller formulation described has been used for all control loops in the simulation studies and on the practical experimental prototype drives. The next chapter focuses on the proposed control strategy for the novel machine and converter topologies presented in this work.

Chapter 7

Converter and Machine Control

7.1 Introduction

One of the main aims of this work is to formulate and evaluate suitable control schemes for the proposed multiphase electronically commutated DC machine topologies. The key challenge in the machine control strategy formulation is to ensure a generic machine control system that enables the multiphase electronically commutated DC machines to mimic the superior operational characteristics and dynamic performance of classical mechanically commutated DC machines. This chapter discusses the proposed machine control schemes applicable to the multiphase electronically commutated DC machine topologies. A generic form of the control scheme which applies to both the two level and multilevel topologies is presented. The proposed control strategy was analysed and simulated in Matlab/Simulink before experimental validation on 15 phase and 24 phase laboratory prototype drives.

Owing to the novelty of the machine and converter topologies presented in this work, no directly applicable control schemes have been reported in literature, as such new suitable schemes derived from the rudiments of well established control schemes are proposed. The main objectives of the proposed control strategy are to:

a): Formulate a control strategy for the electronic commutator to mimic the operation of classical DC machine mechanical commutators for the two-level topology and an equivalent control scheme for the multi-level topology. For electronic commutation of both the two-level and the multi-level topologies,

the control strategy has to be capable of handling three modes of operation for the electronic commutator, i.e. natural commutation, forced commutation and hybrid commutation.

b): Formulate a control strategy for the multiphase electronically commutated DC machine to enable full four quadrant machine operation over the entire torque speed range of the machine.

b): Evaluate the transient, dynamic and steady state performance of the proposed control scheme, firstly via simulation models and finally on experimental laboratory prototype drives.

7.2 Machine Control Schemes Review

A review of existing machine control schemes was initially carried out to assess their suitability for multiphase electronically commutated dc machine topologies. Some of the common drive control schemes in use and widely reported in literature [199],[200], [[189],[189],[211],[212] can be classified according to the topology of the drive converter, i.e. Voltage Source Inverter (VSI) fed drives, Current Source Inverter (CSI) fed drives, or Converter Fed Direct Current Machines.

A literature review of the existing drive control schemes highlighted that there are no existing machine control schemes that can be directly applied to fulfil the above mentioned aims for the new multiphase electronically commutated dc machine topologies. Since the majority of machine control schemes try to mimic the control scheme of classical DC machines owing to their superior dynamic performance, DC machine control scheme was considered a better starting point in the formulation of the control strategy.

Its been well known that the superior dynamic performance of DC machines results from the selective and independent control of the torque and flux producing current components of the machine. The armature control varies the armature current to control the machine torque and the field control varies the field current to control the machine flux. The aim of most ac machine vector control schemes is to achieve similar control dynamic performance as for dc machines. As such, the control scheme

proposed in this work also aims to have selective and independent control of the flux and torque producing components of the machine currents both in transient and steady state conditions.

7.3 Proposed Control Scheme Overview

Having alluded to the superiority of the DC machine control scheme, the control strategy developed in this work has been formulated and partitioned to mimic the classical DC machine control scheme. The control scheme comprises of a field current control scheme for machine flux control and an armature current control scheme for machine torque control. Analysis of the multiphase electronically commutated DC machine topology revealed that two additional control degrees of freedom that do not exist in classical DC machines are available in this machine topology. The first one is the ability to actively control the machine armature current commutation process and commutator operating mode. The second one is the ability to actively control the armature current vector position relative to machine flux. These extra control features are desirable as they permit both positive and negative machine torque control without the need to reverse the armature current as is the case with conventional dc machines which require two back-to-back armature control converters. These extra control variables are incorporated in control scheme formulation.

In the machine control scheme formulation, the goal is to control the machine to maximize the machine torque per ampere for a given operating flux level in steady state. The target applications of this machine are in propulsion systems and renewable power generation. As such, the developed control scheme allows operation either as a speed controlled machine or power controlled machine with dedicated controllers for dc link current, machine flux, field current and electronic commutation control. The machine operating power factor is controlled through the electronic commutator phase control. The machine torque control is achieved by controlling the electronic commutator to inject the dc link current into the appropriate machine armature winding coils at the appropriate rotor position to generate machine torque. The electronic commutator runs at the variable voltage and variable fundamental frequency of the machine, as such the electronic current commutation control has to be synchronised to the rotor

position. Since the electronic commutator is phase controlled, four quadrant machine operation can be achieved by operating the electronic commutator in either rectifying or inverting mode of operation. When motoring, the electronic commutator is inverting DC link power to AC machine power. When generating, the electronic commutator is rectifying machine AC power to DC link power.

7.4 Control Scheme Reference Frame

The control scheme formulated is based on the Field Oriented Control (FOC) [189],[212], [213] which offers independent control of machine flux and torque. Owing to the need to control stator current commutation relative to the machine stator back EMF, the control scheme representation is in the stator flux reference frame which is positioned along the orthogonal **M-T** axis as depicted in figure 7.1. The M–axis is aligned with the stator flux vector and the T-axis is perpendicular to it. The M-axis points in the direction of the stator magnetising current i.e. a component of stator current that produces stator flux and the T-axis points in the direction of torque producing component of the stator current vector. In this representation, the M-T orthogonal axis is offset from the d-axis by the load angle(σ) as shown in figure 7.1. The d-axis is aligned with the rotor pole axis and the q-axis is perpendicular to it. In comparison to the widely used d-q reference frame, the M-T reference frame with stator flux control lends itself well to the control of multiphase electronically commutated DC machines as it conveniently offers the ability to readily control the electronic commutator and machine power factor as will be highlighted later.

For selective influence of machine torque, the stator current vector is positioned in a certain way relative to the stator flux vector through the electronic commutator phase control. In order to maximize machine torque per ampere, the angle between the stator current vector and stator flux vector is maintained as close to 90^0 as possible.

7.4.1 M-T Reference Frame Field Oriented Control

Owing to the universal use of the d-q reference frame, most of the machine parameters are often given in d-q reference frame. To enable controller design in the M-T reference

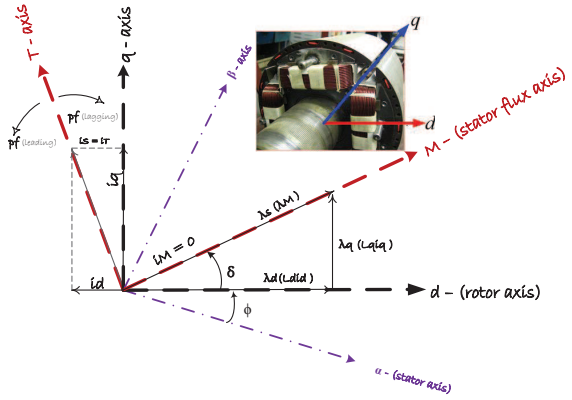

Fig. 7.1 Flux Phasor Diagram Showing the *dq* and *MT* Reference Frames at Unit Power Factor

frame, the machine flux and currents have to be formulated in this reference frame. A similar procedure to that reported in [214] has been adopted to derive the current and flux equations in *M-T* reference frame by using trigonometry to map the *d-q* quantities on to the *M-T* reference frame using the load angle(σ). The *d-q* reference frame from which the equations are derived is shown in figure 7.2.

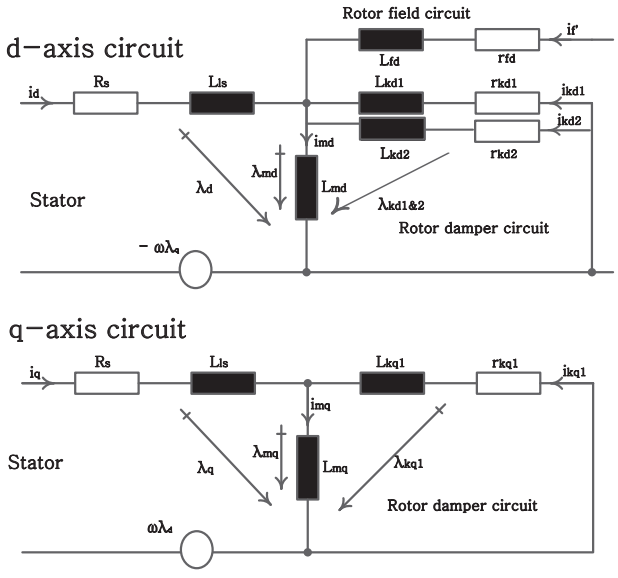

Fig. 7.2 Machine Equivalent Circuit Diagram in dq Reference Frame

In the formulation presented herein, the following notations in figure 7.2 represent machine parameters: *kq, kd* represent the *qd* damper windings, *fd* represent the field winding, λ represent flux linkage; *qs* & *ds* represent stator *qd* variables, v_{md} is the

magnetising branch voltage, qr & dr represent rotor qd variables respectively and ω_r & θ_r are the rotor angular speed and position respectively and the subscript numbers $1,2$ represent damper winding circuit numbers. Figure 5.2 shows a schematic diagram of the dq circuits.

M-T Current & Flux Linkage Components

Firstly, resolving the M-T-axis current components along the d-q-axis to get their corresponding d-q equivalents and expressing the result in matrix form gives;

$$\begin{bmatrix} i_{md} \\ i_{mq} \end{bmatrix} = \begin{bmatrix} \cos(\sigma) & -\sin(\sigma) \\ \sin(\sigma) & \cos(\sigma) \end{bmatrix} \begin{bmatrix} i_M \\ i_T \end{bmatrix} \tag{7.1}$$

where the space phasor of the stator current is given by;

$$i_S = (i_{md} + j i_{mq}) \exp(-j\delta) = (i_M + j i_T) \tag{7.2}$$

The corresponding flux linkage components along the d-q-axis are given by;

$$\lambda_{md} = L_{md}(i_d + i_f^{'} + i_{kD}) = L_{md} i_{md} = L_{md}(i_M \cos(\sigma) - i_T \sin(\sigma)) \tag{7.3}$$

$$\lambda_{mq} = L_{mq}(i_q + i_{kQ}) = L_{mq} i_{mq} = L_{mq}(i_M \sin(\sigma) + i_T \cos(\sigma)) \tag{7.4}$$

The flux linkages along the M-T - axis are obtained by resolving (7.3) and (7.4) flux linkage components along the M-T - axis and summing up the respective terms to give;

$$\lambda_M = \lambda_{md} \cos(\sigma) + \lambda_{mq} \sin(\sigma) + L_{ls} i_M \tag{7.5}$$

$$\lambda_T = -\lambda_{md} \sin(\sigma) + \lambda_{mq} \cos(\sigma) + L_{ls} i_T \tag{7.6}$$

The field flux linkage is given by;

$$\lambda_f^{'} = -\lambda_{md} + L_{lf} i_f^{'} \tag{7.7}$$

Its clear from the above analysis that the equations for the *d-q* components can be readily obtained by substituting $\sigma = 0$ in (7.3) to (7.6).

Machine Electromagnetic Torque

An expression of the machine electromagnetic torque can be readily obtained from the cross product of the stator flux linkage and current space phasors [189]. For this multiphase machine/converter topology with N stator phases and P pole pairs , an expression of the developed electromagnetic torque in the chosen *M-T* - axis reference frame can be obtained by the cross product of the flux linkage and the *M-T* - axis currents as;

$$T_e = \frac{N}{2}\frac{P}{2}(\lambda_M i_T - \lambda_T i_M) \tag{7.8}$$

It can be seen from (7.8) that in order to maximize the torque $\lambda_T = 0$ which implies that $\lambda_M = \lambda_s$ the stator flux linkage. This condition highlights the decoupling and independent control of machine torque via i_T and machine stator flux via λ_s achievable in this reference frame representation of the control structure. For rapid torque changes, it can be assumed that owing to the large time constant of the machine flux circuit, the machine torque can be rapidly changed through rapid changes in i_T.This is readily achievable in this drive topology since the magnitude of i_T is controlled by a separate current source converter with a control bandwidth that is order of magnitude faster.

7.5 Design of Regulators

To formulate the control loops for the proposed machine and converter topology, the machine subsystems are split into elementary transfer functions to simplify the controller design. Analysis of the subsystem transfer functions of the control loops revealed that all the transfer functions of the controlled subsystems can be regarded as first order systems. As such, the first order polynomial RST controller design structure discussed in chapter 6 is applied to the major control loops. The two main tuning parameters for the controllers that sets the desired dynamic performance required are

the controller bandwidth ω and the desired controller damping ζ. The overall control scheme is shown in figure 7.3.

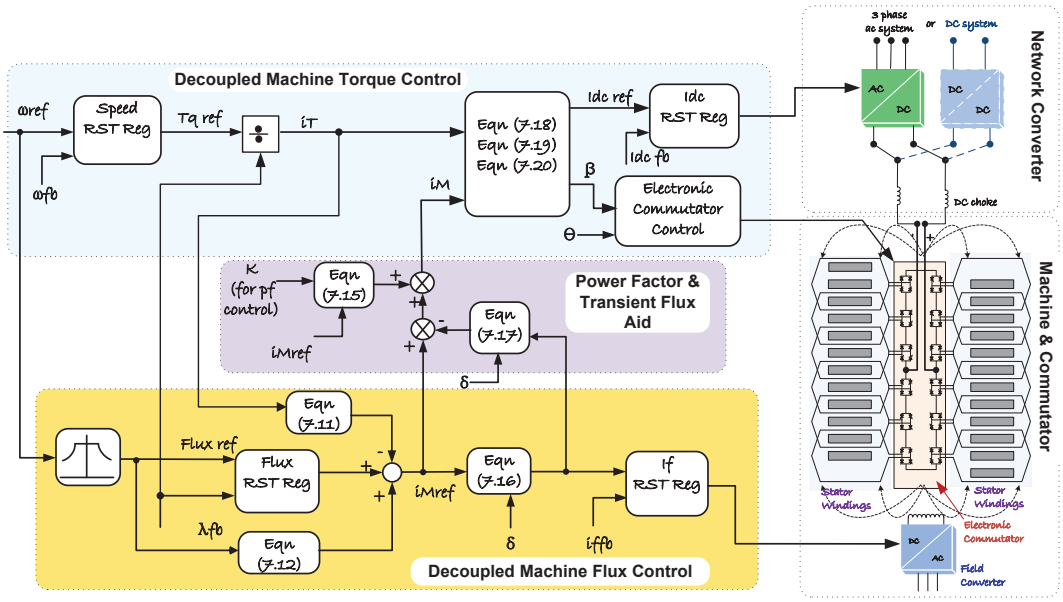

Fig. 7.3 Simplified Schematic of Proposed Control Strategy

7.5.1 Flux and Field Current Regulators

In addition to selective torque control via the outer speed control loop which generated a machine torque reference, the machine control has been formulated to also enable selective and independent control of machine flux. An outer control loop regulates the machine flux to its rated value up to base speed and weakens the flux above base speed. The flux controller outputs a field current reference for the field current controller which regulates the machine field current. The inner field current control loop has a higher control bandwidth than the outer flux control loop. Although wound rotor machines have been considered in this study, the proposed control scheme is equally applicable to permanent magnet machines. In this control formulation, the magnetising current reference is generated by two components; one is a calculated open loop current reference $i^*_{M_{ref}}$ and the other is the output of a flux controller $i^*_{M_{ref_\Delta}}$. The flux and field current control scheme is shown in figure 7.3, the equations implemented in this scheme are derives in the following analysis.

Open Loop Current Reference

The open loop magnetising current reference $i^*_{M_{ref}}$ is given by dividing the flux reference term $\lambda_{M_{ref}}$ by the magnetising inductance. An expression for this current reference can be derived from the expression of the magnetising flux. This is obtained by substituting (7.3) and (7.4) in the expression of the magnetising flux linkage (7.5) and simplifying the resulting expression to yield;

$$\lambda_M = ((L_{md} - L_{mq})\cos^2(\sigma) + L_{mq} + L_{ls})i_M + \frac{(L_{mq} - L_{md})}{2}\sin(2\sigma)i_T \tag{7.9}$$

From (7.9) an expression of the magnetising current reference can be obtained as;

$$i^*_{M_{ref}} = \frac{\lambda_{M_{ref}}}{(L_{md} - L_{mq})\cos^2(\sigma) + L_{mq} + L_{ls}} - \frac{\frac{(L_{mq} - L_{md})}{2}\sin(2\sigma)}{(L_{md} - L_{mq})\cos^2(\sigma) + L_{mq} + L_{ls}}i_T \tag{7.10}$$

The second term in (7.10) is a cross coupling term from the T-axis.

$$i^*_{M_{ref_{ff}}} = -\frac{\frac{(L_{mq} - L_{md})}{2}\sin(2\sigma)}{(L_{md} - L_{mq})\cos^2(\sigma) + L_{mq} + L_{ls}}i_T \tag{7.11}$$

This term can be neglected if high transient dynamic performance is not required as the cross coupling error introduced can be eliminated by the flux controller in steady state conditions. However, if high transient dynamic performance is required, this cross coupling term can be added as a feed-forward term to the overall magnetising current reference as depicted in figure 7.3.

Ignoring the second term, the magnetising current reference can be computed based on the desired magnetising flux reference profile using the first term of (7.10) as:

$$i^*_{M_{ref}} = \frac{\lambda_{M_{ref}}}{(L_{md} - L_{mq})\cos^2(\sigma) + L_{mq} + L_{ls}} \tag{7.12}$$

It can be seen from (7.12) that at zero load the magnetising current reference is given by $i^*_{M_{ref}} = \frac{\lambda_{M_{ref}}}{L_{md} + L_{ls}}$. The load angle σ term accounts for the armature reaction effect when load is applied. It can be argued that with the above equation defining the field current reference to account for load changes there is no need for an outer

flux controller. However, to account for errors due to machine parameter variations with operating conditions and also during transient conditions, a flux controller was deemed necessary.

7.5.2 Flux Controller

The flux circuit can be reduced through approximation to the first order lag element. Some simplifying assumptions have been made by neglecting the i_d and i_f coupling derivative current terms. This simplification is reasonable owing to the large dynamic differences of these coupling terms [215], as such, their effect can be considered to be far less dominant. By neglecting the cross coupling term in the flux equation, the transfer function of the flux regulator is approximated by $G(s) = \frac{L_{md}}{\tau_D s+1}$, where $\tau_D = \frac{L_{kD}}{R_{kD}}$. The resultant system transfer function steady state gain $k = \frac{L_{md}}{\tau_D}$ and open loop system pole $a_0 = \frac{1}{\tau_D}$ are used in calculating the RST controller polynomials as discussed in chapter 6. The stator flux generates a current reference component $i^*_{M_{ref_\Delta}}$.

Total Magnetising Current Reference

The total magnetising current reference for the M-T reference frame is given by the sum of the current reference components described above including the optional cross coupling feed forward term. A variable $\hat{k}$ ranging from $0 \leq \hat{k} \leq 1$ can be defined such that, when $\hat{k} = 0$ cross coupling feed-forward is inhibited and $\hat{k} = 1$ for applying full compensation for cross coupling. Thus, the magnetising current reference along the M-axis can be expressed as;

$$i_{M_{ref}} = i^*_{M_{ref}} + i^*_{M_{ref_\Delta}} + \hat{k} i^*_{M_{ref_{ff}}} \tag{7.13}$$

This magnetising current can be wholly provided through the rotor circuit or partly through the stator circuit. A factor ε can be defined such that the respective current components provided through the rotor ($i_{M_{ref_\mathbf{r}}}$) and stator ($i_{M_{ref_\mathbf{s}}}$) are given as;

$$i_{M_{ref_\mathbf{r}}} = (1 - |\varepsilon|) i_{M_{ref}} \tag{7.14}$$

$$i_{M_{ref_{\mathbf{s}}}} = \varepsilon i_{M_{ref}} \tag{7.15}$$

When $\varepsilon < 0$ the machine operates with a leading power factor, when $\varepsilon > 0$ the machine operates with a lagging power factor, when $\varepsilon = 0$ the machine operates at unit power factor. Simulation and experimental measurements have shown that the operating power factor can be regulated to the desired operating targets using ε as defined by (7.14) and (7.15).

Steady State Operation

From the preceding analysis, its clear that to maximize machine torque under steady state conditions, ε should be zero, i.e. stator magnetising current component ($i_{M_{ref_{\mathbf{s}}}}$) is zero and $i_{M_{ref}} = i_{M_{ref_{\mathbf{r}}}}$. Its clear that this condition implies that stator current space phasor is entirely torque producing (i.e. i_T) and is co-phasal with the stator voltage space phasor. This assures the unit power factor condition of the machine at steady state operating conditions. This is one advantage of formulating the control scheme in the stator reference frame as stator voltage feedback signals can be directly employed and processed to directly generate the electronic commutator firing synchronisation angle.

Since the field current is co-phasal with the d-axis, to account for the shift in stator flux vector position (σ) in the M-T frame relative to the field flux vector d-q position under load, the field current reference term can be computed by resolving the magnetising current reference along the field axis (d-axis) to give;

$$i_{f_{ref}} = \frac{i_{M_{ref}}}{\cos\sigma} \tag{7.16}$$

Transient State Operation

Under transient conditions, owing to the typically large rotor time constant of wound rotor machines, the response of the field current is inherently slow bearing in mind the forcing voltage capability of the field converter has a direct impact on cost and size. This imposes a limit on the capability of the field converter to rapidly force rotor field winding current change. On the other hand, the machine stator circuit time constant is

typically small. The strategy adopted exploits this stator circuit attribute to enhance the transient performance of the proposed control scheme by transiently providing a component of the machine magnetising current ($i_{M_{ref_s}}$) that is co-phasal with stator flux vector along the M-axis on the M-T frame. Analysis of the governing equations shows that during the transients, when the field current is not yet fully established, the transient magnitude of magnetising component of the stator current required can be expressed as;

$$i_M = i_{M_{ref_s}} - i_{f_{fb}} \cos\sigma \tag{7.17}$$

where $i_{f_{fb}}$ if the measured field current feedback signal. The technique to improve transient performance by stator current injection is not new, in fact, this has been successfully applied to Cyclo-converter fed drives [27]. Its clear from the above analysis that a penalty of this strategy is that under these conditions $\varepsilon \neq 1$ and the power factor deviates from unity. However, bearing in mind that dynamic performance is given priority over power factor control during transient conditions, this penalty is not significant. Infact, when steady state condition is attained, the entire magnetising current will be provided by the field current.

Its clear from the above analysis that, for machines with small short circuit ratios, i.e. machines that operate at large values of load angles, control changes to the field current will have less effect on the resultant flux magnitude, i.e. the bigger the load angle the large the proportion of field current required to effect flux change, as can be inferred from the phasor diagram of figure 7.1. Under these conditions, the stator current is given by the vector sum of the torque producing component i_T and flux producing component i_M.

The experimental prototype drive has shown that damper windings have a significant beneficial effect on the behaviour of multiphase electronically commutated DC machines with regard to the dynamics of the torque control, the flux and field control and electronic commutation process. With damper windings, the control of the machine torque via stator current is somewhat decoupled from the motion of the flux vector. This decoupling is because the damper winding compensates for the magnetisation caused by the transient stator current, as a result, the flux vector moves

slowly from its position relative to the rotor position [216]. Thus, during rapid transient torque changes, only leakage inductances (not in addition to the main inductance), has to be re-magnetised. Damper windings have also been shown in the experimental validation tests to help in reducing the machine commutating inductances and thus aid rapid stator phase current commutation.

7.5.3 Field Current Control

The field circuit subsystem transfer function is given $G(s) = \frac{i_f}{v_f} = \frac{1}{sL_f+R_f}$, where v_f if the voltage applied by the field converter. The field plant parameters used in the RST controller design are the open loop plant gain $k = \frac{1}{L_f}$ and open loop system pole $a_0 = \frac{R_f}{L_f}$ as depicted in figure 7.4. As highlighted in the preceding analysis, the demanded field current control reference for the machine control is computed from (7.16).

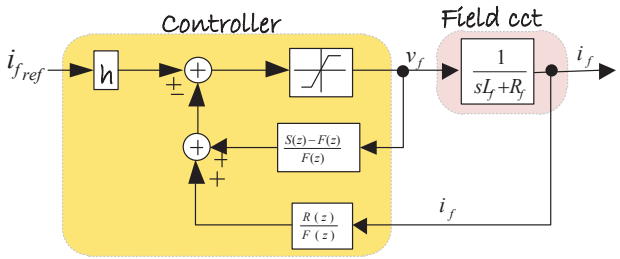

Fig. 7.4 Simplified Schematic of the Field Current Controller

Figure 7.5 shows simulation results of the flux and field current control loops for machine speed accelerating from standstill to negative full speed and reversal to full positive machine speed. Both the flux regulator and field current regulator successfully tracks their respective references.

7.5.4 Speed Control

The speed control loop regulates the machine speed and generates the torque reference. The torque producing component of the stator current i_T is derived from the speed controller output torque reference command by dividing it by the machine flux magnitude.

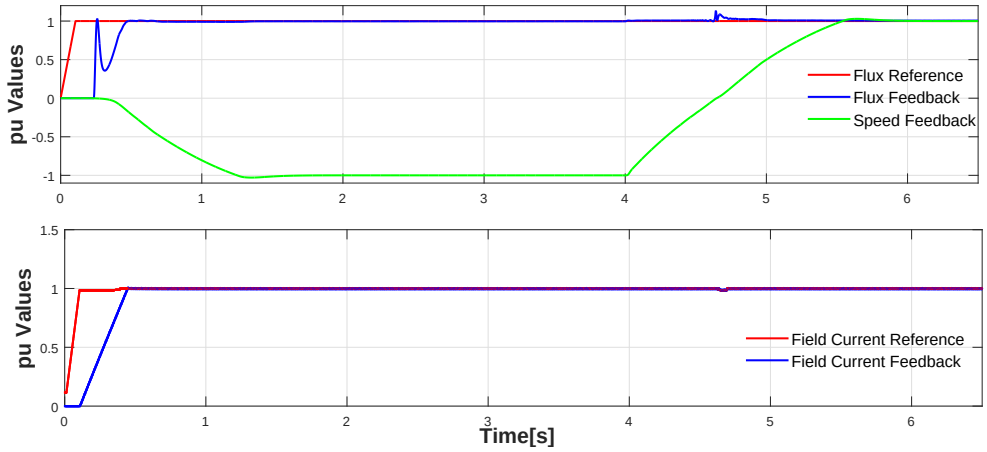

Fig. 7.5 Simulation of Control Scheme Machine Full Speed Reversal: Flux and Field Current Control

i_T The dc link current reference can be derived from the vector sum of the torque and flux producing components of the currents i_T and i_M and expressed as;

$$i_{dc_{ref}} = \sqrt{i_M^2 + i_T^2} \tag{7.18}$$

and the angle at which the current is injected into the machine relative to the phase voltage is given by;

$$\beta = \arccos\left(\frac{i_T}{i_{dc}}\right) \tag{7.19}$$

The equation for the mechanical subsystem is governed by $J\frac{d\omega}{dt} + F\omega = T_e - T_m$; where J is the total inertia of the rotating machine parts in $kg.m^2$, F is friction coefficient in $N.m/(rad/s)$, T_e is electromagnetic torque and T_m is the mechanical torque. Owing to the polygonal winding function of the Active Stator machines, the dc current injected into the machine splits into two parallel parts such that each machine phase carries half the injected dc link current. From the differential equation of the mechanical system and recalling (7.8) and mapping onto the M-T reference frame with unit power factor, the plant transfer function for the speed controller can be expressed as;

$$G(s) = \frac{\omega(s)}{i_T(s)} = \frac{N}{2}\frac{P}{2}\lambda_M(s)\frac{1}{sJ+F} = k_{Tq}\lambda_M(s)\frac{1}{sJ+F} \tag{7.20}$$

where $k_{Tq} = (\frac{N}{2}\frac{P}{2})$, N and P are the number of stator phases and machine pole pairs respectively. For the speed control RST controller design, the system (plant) parameters

required in for the computation of the controller polynomials are the steady state system gain $k = \frac{1}{J}$ and the system open loop pole $a_0 = \frac{F}{J}$.

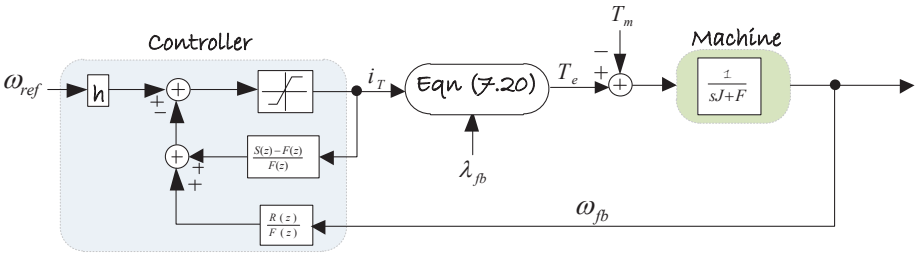

Fig. 7.6 Simplified Speed Regulator Schematic Diagram

Figure 7.7 and figure 7.8 show experimental measurement of the implemented speed controller to step changes and speed ramp up measured on a 24 phase machine prototype machine. Since the speed control loop is an outer control loop with cascaded inner dc link current and electronic commutator control loops, the figures shows that the overall control strategy proposed yields good results.

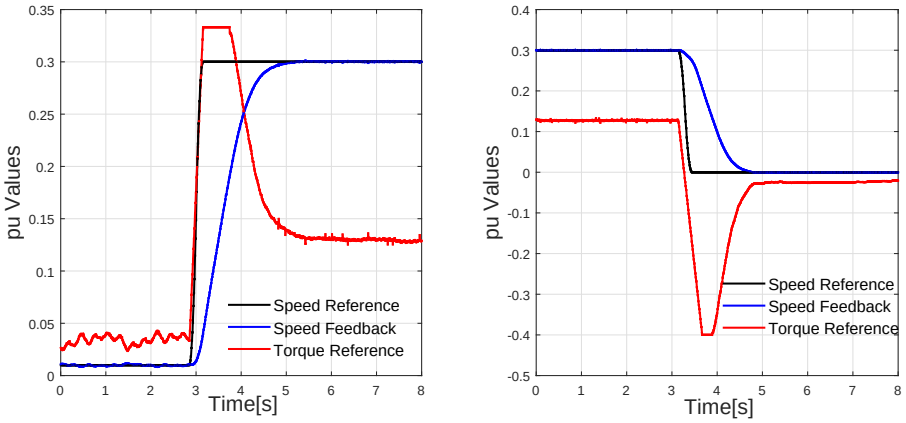

Fig. 7.7 Experimental Measurement of Speed Controller Step Response from Zero to 0.3pu and 0.3pu to Zero Speed

7.5.5 DC Link Current Control

For four quadrant operation of the Active Stator machine, owing to its current source type topology the current injected in the machine is the dc link current which is

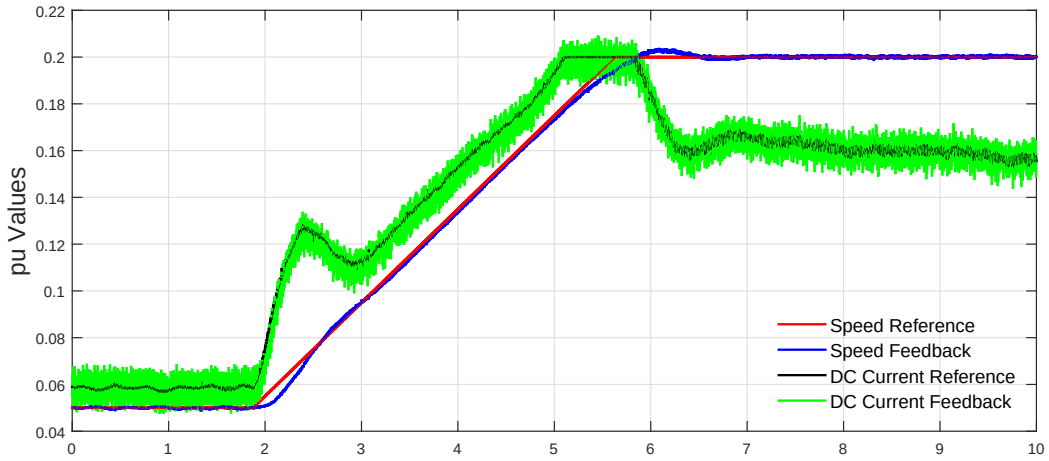

Fig. 7.8 Experimental Measurement of Speed Controller Ramp from Zero to 0.2pu

regulated by a separate dc link current controller. The dc link current reference given by 7.18 sets the demanded machine current. Depending on the machine operating power factor, this current reference is a vector sum of the magnetising and torque producing components of the machine stator current. Active Stator machines can be AC or DC fed, hence figure (7.3) highlights both options.

To prove the good transient and dynamic performance of the proposed control scheme, in terms of speed control, dc link current control and electronic commutator control, an onerous machine fast quadrant transition test at fixed machine speed was done on the prototype machine. In this experiment, the machine torque was rapidly changes from one quadrant to the other whilst the machine speed was held constant via the load machine. Figure 7.9 shows measured results for full torque reversal from 1.0 pu to -1.0 pu vice versa in one second, highlighting the robust dynamic performance of the proposed control scheme. It can be seen that the dc link current controller successfully tracks its reference signal and the electronic commutator control successfully facilitates quadrant transitions by reversing the dc link voltage polarity whilst remaining synchronised to rotor position vector all the time.

7.5.6 Flux and Load Angle Estimation

The machine flux feedback & load angle signals employed in the presented control scheme were derived from the well established machine current and voltage models

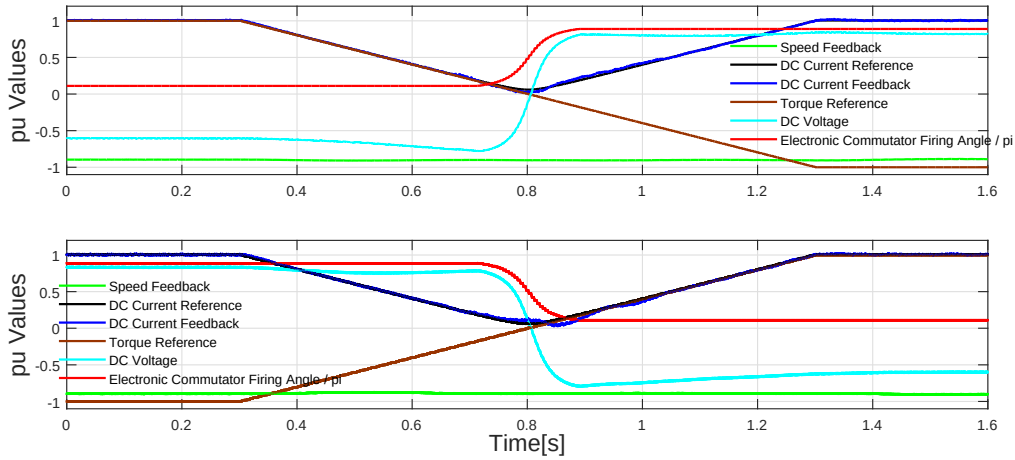

Fig. 7.9 Experimental Measurement of Machine Torque Transitions at Fixed Shaft Speed

[189],[217] but with some subtle modifications to account for the new topology features such as high number of stator phases and electronic current commutation. The derivation of these models will not be repeated here, only the subtle features specific to this topology will be highlighted. The machine current and voltage models were implemented in $\alpha - \beta$ reference frame using Clarke's transform [199]. The machine current model is used at low speeds, below 2Hz, where the voltage model is inaccurate due to significant stator ohmic voltage drop which depend on machine operating conditions and also due to the fact that the voltage signals diminish as the speed approaches zero.

Machine Phase Voltage Measurements

Owing to the high number of stator phases inherent in this topology, the cost of implementing the control scheme if all stator phase voltages and currents are measured can be very high. With this in mind, the machine stator phase number was chosen to be a multiple of three. Imposing this constraint leads to a reduction of the required machine voltage measurement signals. Infact, only three voltage measurements that result in a balanced three phase set for the overall machine are necessary and these can be easily obtained by positioning the three voltage sensors on the appropriate machine phases. For example with a 15 phase machine, three differential voltage measurement between phases $V_{(1-6)}$, $V_{(6-11)}$, and $V_{(11-1)}$, can be used as depicted

in figure 7.10 which shows differential voltage measurement on a 15 phase machine under load conditions. Simulations and experimental measurements have confirmed that this approach yields good control performance as will be seen in the simulation and measured results later.

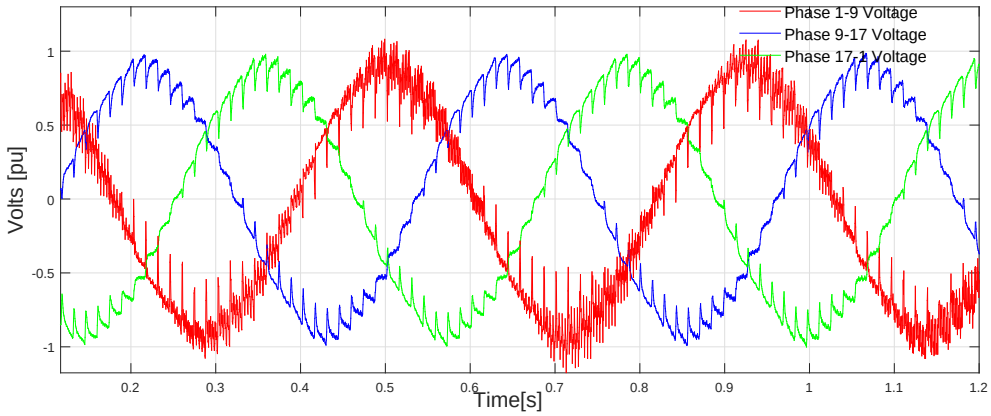

Fig. 7.10 Balanced 3 Phase Voltages Set Derived from Measuring Three Voltages on a 15 Phase Machine

Machine Phase Current Measurements

Similar to the machine voltage measurement feedback signals, owing to the large number of stator phases, there is no need for measuring individual stator phase currents for control purposes. Simplifying assumptions have been made in the formulation of the control scheme to avoid the cost penalty of measuring all stator phase currents. Owing to the peculiar nature of this machine topology where the machine dc link current splits equally into two around the machine polygonal winding, the individual machine phase currents can be easily computed from the measured dc link current and electronic commutator operating state. As such, the individual stator phase currents of this multiphase machine topology are not measured for control purposes. Instead, the dc link current is measured and the $\alpha - \beta$ current components used in the machine voltage and current models are derived from the M-T reference frame. Furthermore, simulation and experimental results have also confirmed that measurement of the dc link current rather than individual phase currents is sufficient to enable fault detection when used in conjunction with electronic commutator clamp capacitor voltage measurements.

7.6 Simulated and Measured Control Performance

The control system describe has been successfully implemented in C-programming language for direct porting to industrial control hardware. The same source code has also been directly imported into the drive simulation models using Matlab/Simulink S-functions thereby allowing identical source code to be used in the simulation models and the intended control hardware. This also enabled easy debugging of the implemented C-code as test vectors can be easily defined and run as simulation scripts to fully excise the intended functionality and identify errors before its applied on a physical system.

Simulation studies and experimental tests conducted to characterise the dynamic and steady state performance of the proposed control scheme demonstrated the validity of the proposed scheme. Figure 7.11, shows simulation results of the proposed control scheme for machine with large inertia load accelerating from standstill for full negative speed and then reversing the shaft speed to full positive speed. Figure 7.12 shows the corresponding electronic commutator phase 1 current and machine phase current and voltage waveforms and a zoom of these signals. Quadrant changes are achieved via electronic commutator phase control which acts to reverse the polarity of the dc link voltage whilst maintain unipolar current direction as shown in figure 7.13.

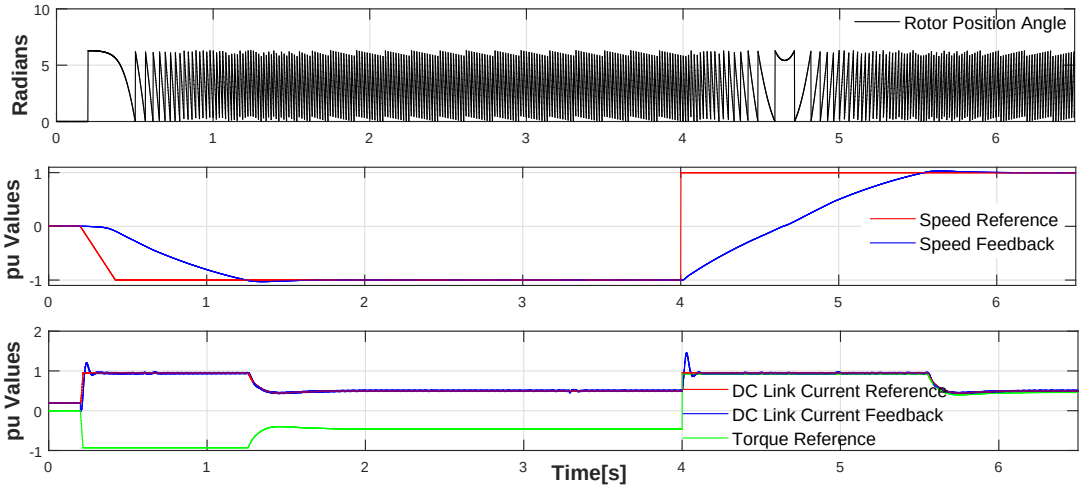

Fig. 7.11 Simulation of Control Scheme Machine Full Speed Reversal

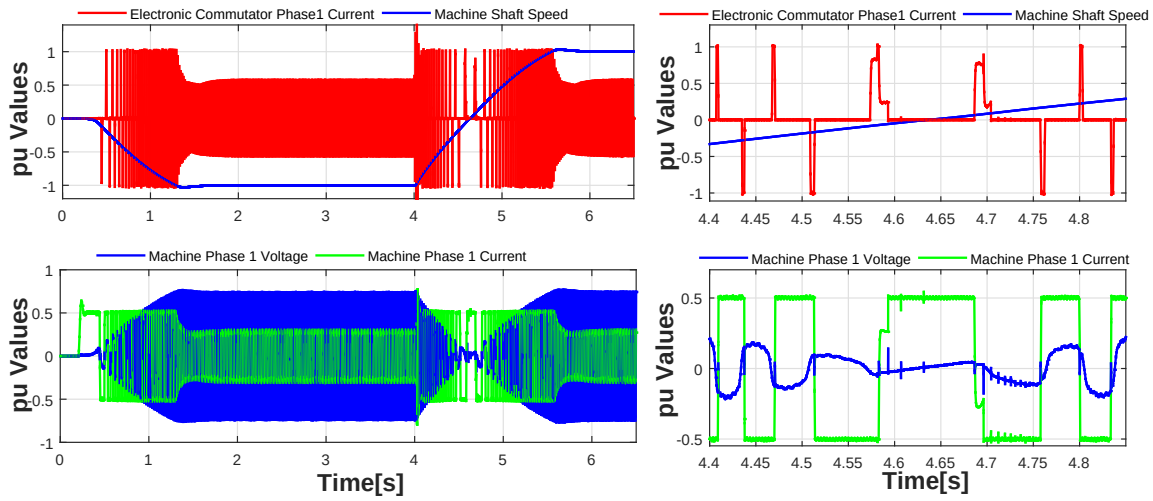

Fig. 7.12 Simulation of Machine & Electronic Commutator Phase Voltages and Current During Machine Full Speed Reversal

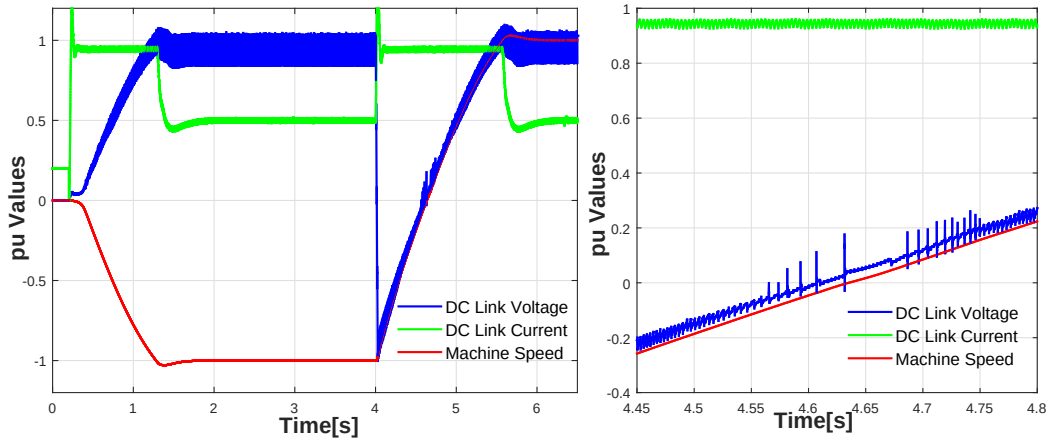

Fig. 7.13 Simulation of DC Link Voltage and Current During Machine Full Speed Reversal

Figure 7.14 and figure 7.15 shows experimental measurement taken on a 24 phase prototype machine for $\pm$ 0.5 pu speed reversal, illustrating the robustness of the electronic commutator control, dc link current control and speed control loops.

Figure 7.16 shows experimental measurement taken on a 15 phase prototype machine for $\pm$ 0.1 pu speed reversal, illustrating the interleaving electronic commutator control of the switching devices that connect the machine phases to the positive and negative dc link terminals discussed in earlier chapters which is essential for avoiding circulating currents in the machine polygonal winding of odd stator phase number machines.

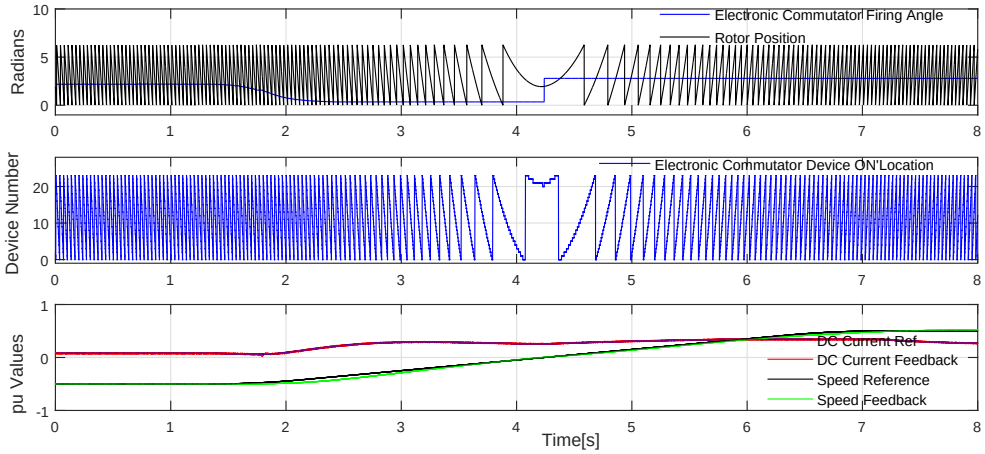

Fig. 7.14 Experimental Measurement of Negative to Positive Speed Reversal on a 24 Phase Machine

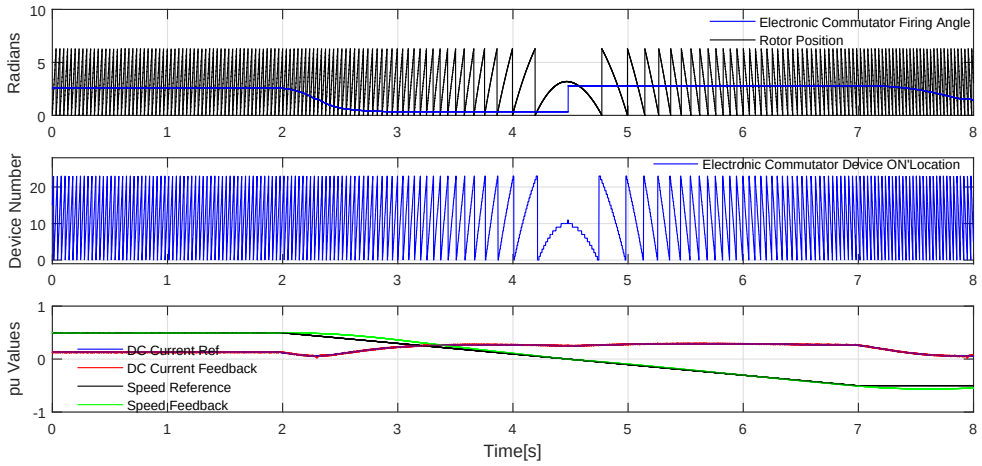

Fig. 7.15 Experimental Measurement of Positive to Negative Speed Reversal on a 24 Phase Machine

7.7 Discussion

The proposed control scheme in the MT-reference frame can be interpreted in terms of the load angle control. In this control scheme, the machine flux is kept constant by the action of an open loop field current reference together with a closed loop flux regulator. This implies that ratio of the machine voltage to frequency is kept constant i.e. ($\lambda = \frac{v}{\omega}$). From figure 7.1, the q-axis flux is given by;

$$\lambda_q = L_q(i_M \sin(\delta) + i_T \cos(\delta)) \tag{7.21}$$

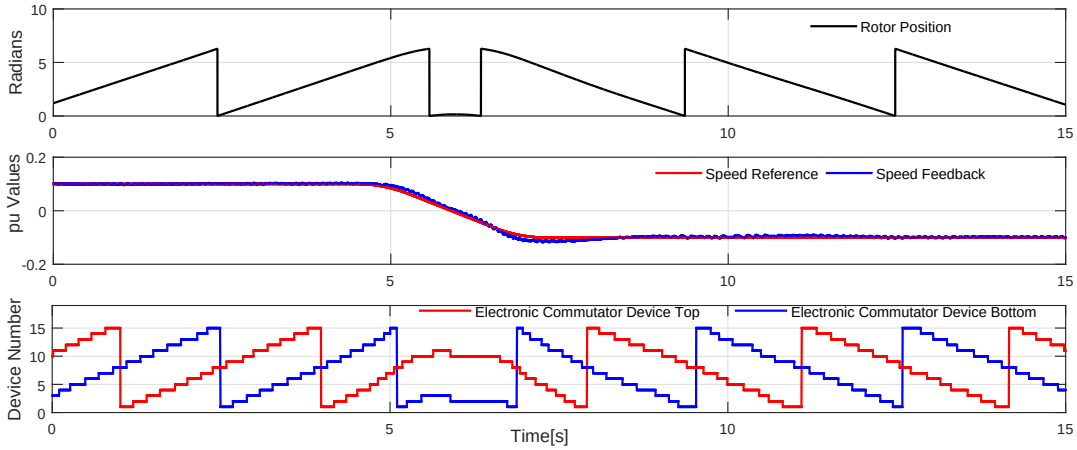

Fig. 7.16 Experimental Measurement of Positive to Negative Speed Reversal on a 15 Phase Machine

Bearing in mind the flux vector is along the M axis, the q axis component can also be expressed as;

$$\lambda_q = \frac{v}{\omega}\sin(\delta) \tag{7.22}$$

giving;

$$\lambda_q = L_q(i_M \sin(\delta) + i_T \cos(\delta)) = \frac{v}{\omega}\sin(\delta) \tag{7.23}$$

Thus;

$$v\sin(\delta) = X_q(i_M \sin(\delta) + i_T \cos(\delta)) \tag{7.24}$$

dividing (7.24) by $\cos(\delta)$ and rearranging yields;

$$\tan(\delta) = \frac{i_T X_q}{v - i_M X_q} = \frac{i_{dc}\cos(\delta)X_q}{v - i_{dc}\sin(\delta)X_q} \tag{7.25}$$

It can be seen that (7.25) is the equation of the synchronous machine, bearing in mind i_{dc} is the same as the machine current.

7.8 Summary

This chapter has introduced and discussed the proposed control strategy formulation for controlling the multiphase electronically commutated DC machine topology. The

proposed control scheme has been successfully implemented in Matlab/Simulink to control the new machine and converter topology. the scheme has been experimentally validated on two prototype machines, a 24 phase machine and a 15 phase machine. The control scheme successfully demonstrated the three key objectives highlighted earlier in the introduction of this chapter regarding; (a) mimicking the operation of classical DC machine mechanical commutators, (b) enabling full four quadrant machine operation over the entire torque speed range and (c) ensuring robust transient, dynamic and steady state performance. Details of the design and implementation of the laboratory experimental prototype machines and their electronic commutators is discussed in the following chapter before the detailed experimental results are presented and some concluding remarks given.

Chapter 8

Experimental Prototype Drives Design and Implementation

8.1 Introduction

The machine and converter topologies discussed and presented in this work have so far been analysed using simulation models and some measured results have been presented also. To gain full confidence in the viability of the proposed machine and converter topologies, practical demonstration laboratory test drives had to be design and built to enable experimental validation. Owing to time and financial constraints, only two topologies were practically validated, namely; (a) the multiphase two level topology with an even number of stator phases and (b) the multiphase two level topology with an odd number of stator phases. This chapter summarises the design, implementation and experimental setup of the two experimental laboratory rigs used for the practical validation work.

8.2 Aims of Experimental Laboratory Prototype Drives

The experimental test drives were specifically designed as proof of concept drives, with the following specific aims:

(a) To experimentally prove the practical viability of the proposed multiphase machine and electronic commutation converter topologies.

(b) To develop and validate proposed control strategies for electronic commutation of the multiphase machine topologies, particularly the electronic commutator power electronic topology and how its actively controlled to mimic the behaviour of mechanical commutation process of conventional dc machines .

(c) To develop and validate the overall drive control strategies that ensure full four quadrant operation of the proposed multiphase machine and converter topologies.

(d) To fully characterise the transient, dynamic and steady state performance of the overall drive system, i.e. machine, power electronic converter and control system, over the entire drive torque/speed operating range.

(e) To gain a deeper understanding of the machine and converter topology behaviour, thus enabling the development of design tools that facilitate optimal machine and converter designs.

(f) To explore the practical possibilities and challenges of integrating the machine and its associated power electronics as a single unit.

(g) To characterise the performance benefits of even and odd number of stator phases and assess the impact of commutating inductance and machine armature reaction on the overall performance of the drive.

(h) To investigate fault tolerance of the proposed drive system.

8.3 Experimental Prototype Drives Setup

Each of the two experimental test drive laboratory rigs were designed to enable full characterisation of the transient and dynamic performance of the machine and converter topologies for both motoring and generating quadrants. The circuit layout of each of the laboratory test rigs included; machine and converter under test, its associated network converter for interfacing to the ac grid, a load machine and its associated four quadrant regenerative inverter and active front end converter. Figure 8.1 shows the test rigs general arrangement. Owing to the power ratings of the laboratory test

rigs, the back to back fully regenerative configuration was adopted to enable power recirculation between the load drive and the drive under test, thereby minimizing power consumption from the ac grid. With this setup, only a small fraction of the rated power is drawn from the ac grid to compensate for the drive system losses.

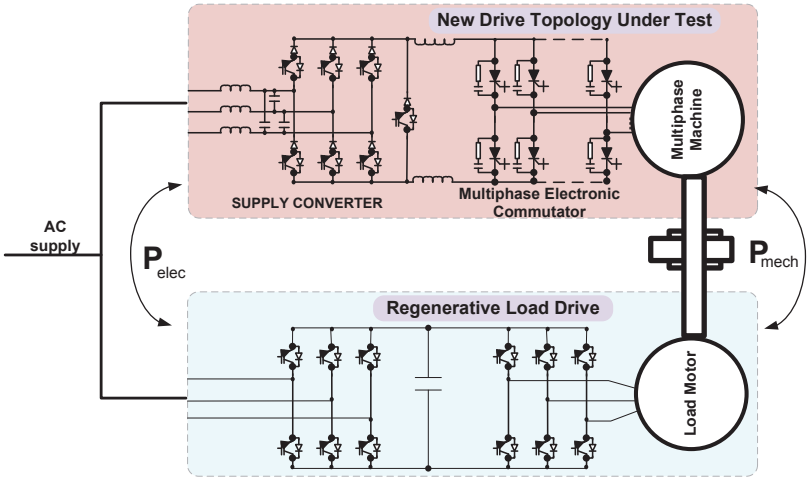

Fig. 8.1 Experimental Laboratory Test Drive Setup.

8.4 Even Stator Phase Number Test Rig

The first laboratory test drive was designed to enable validation of the even numbered multiphase two level machine and converter topology. In this test rig, no particular attention was paid to the electromechanical packaging and integration of the converter with the machine. The main aim was for proving the viability of the proposed machine and electronic commutator topology and its associated control strategy. Details of the drive under test and its load drive are summarized in the following paragraphs.

8.4.1 24 Phase Machine

In addition to validating the topology, the multiphase machine was designed to explore some of the concepts that have been highlighted in the earlier discussions, such as the diminished impact of harmonics on machine performance if the stator phase number is sufficiently high. In this case 24 stator phases were deemed sufficient to highlight this machine feature. The prototype machine rating is summarized below:

1. Machine:
    - Machine rated Power = 150 kW
    - Machine stator phase number = 24 $phases$
    - Machine rated stator frequency = 60 Hz (selected based on machine pole number to enable four quadrant back to back operation with standard 60Hz load machine).
    - Machine rotor type = 4 $saliant \quad pole, \quad wound \quad rotor$
    - Machine rated field current = 32 A
    - Machine Commutating Inductance = 32 μH
    - Machine rated phase voltage = 42 $V \quad rms$

In the discussion presented earlier, it was highlighted that improving power density and reducing overall drive footprint was desirable. This prototype machine was designed to further explore some of the multiphase machine topology attributes that can enhance the machine and converter power density and yield overall footprint reduction. The two features that were explored in this design included; (a) exploiting the multiphase topology immunity to detrimental effects of low order harmonics alluded to in the theory presented in earlier chapters and (b) minimisation of machine commutating inductance to facilitate compact power electronics designs. Figure 8.2 shows pictures of the experimental 24 phase machine and the load machine.

Trapezoidal Machine Phase Voltage

Having alluded to the fact that increasing the stator phase number shifts the undesirable machine space and time harmonics to higher orders where their undesirable impact on machine performance diminish with increasing stator phase number as illustrated by (2.10), this feature was exploited to improve the machine power density. Instead of designing the machine to have a sinusoidal stator phase winding and sinusoidal airgap flux, the machine was designed to give a trapezoidal stator phase back emf voltage waveform which is rich in low order harmonics. In this machine and converter topology, increased air gap shear stress is obtained by also employing a trapezoidal armature current waveform, a trapezoidal air-gap flux density distribution and a near ideal phase displacement between stator MMF and field axes.

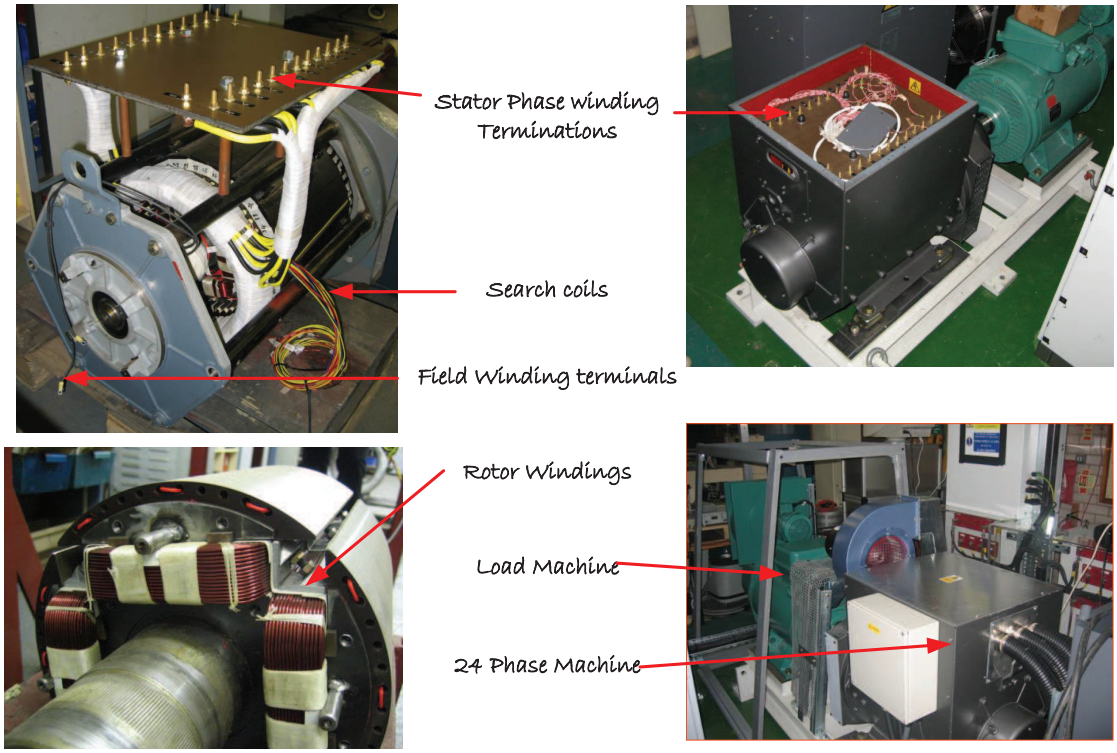

Fig. 8.2 Picture of the 24 Phase Machine and its Load Drive.

The use of a trapezoidal flux distribution and corresponding armature/stator current will maximise torque density, but will also have a significant beneficial effect upon commutation. By maximising the machine back emf E at the end of a conduction period and the start of the commutation, the overlap angle μ may be reduced, thereby allowing the commutation to be delayed to more closely approach the ideal of "brush axis set to the Geometric Neutral Axis (GNA)" of conventional brushed mechanical commutated machines . The more square the flux distribution can be made, the better. Approximately constant $\int Edt$ is required to commutate a given armature current and the required $\int Edt$ is approximately proportional to armature current.

Trapezoidal stator machine voltage waveforms lead to increased machine power output due to the trapezoidal airgap flux waveform compared to machines with sinusoidal airgap flux. This is illustrated in Figure 8.3 which shows the theoretical and measured stator waveform on this experimental prototype 24 phase machine. This highlights the advantage of trapezoidal airgap flux compared to sinusoidal airgap flux, as seen by a 25% volts seconds area increase compared to the sinusoidal designs. A trapezoidal distribution of the air-gap flux density yields a smaller and lighter machine

compared to traditional machines with sinusoidal distribution due to better utilisation of machine iron. Trapezoidal airgap machine design also facilitates machine phase coil winding as simple fully pitched winding can be used. Fully pitched stator phase windings were employed in this prototype machine design. Figure 8.4 shows the measured

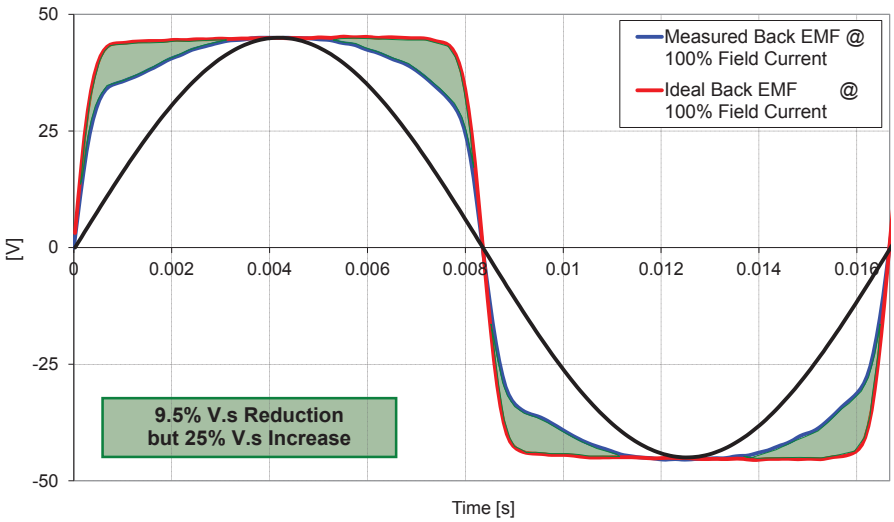

Fig. 8.3 Theoretical and Measured Trapezoidal Machine Phase Back EMF & Comparison with Sinusoidal Waveform.

variation of the 24 phase prototype machine phase trapezoidal back emf for different machine field current excitation levels. For this prototype machine, the measured machine phase voltages appear to be non symmetric at high levels of excitation. This was attributed to a combination of the rotor bore not being perfectly round and also also rotor pole tip saturation, which accounted for circa 9% reduction in volts seconds area in comparison to the theoretical case..

Machine Commutating Inductance

Another design feature that was explored in this experimental machine design was investigating some of the possible ways of minimizing machine commutating inductance by encapsulating the machine rotor in a damper cage in the form of a cylindrical rotor

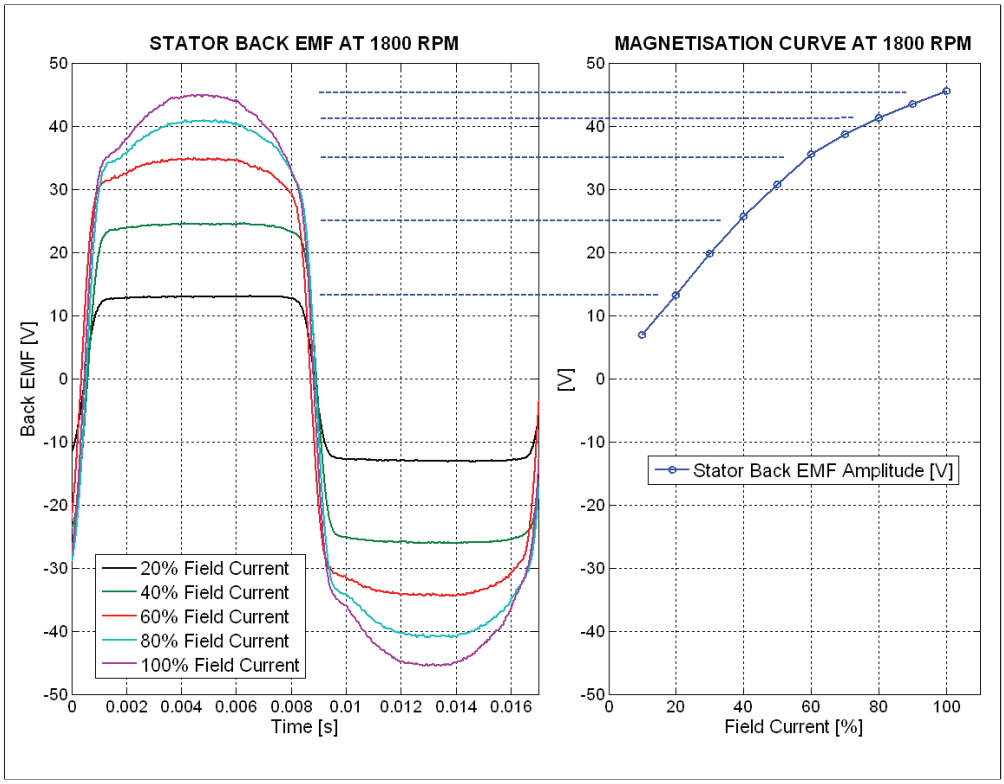

Fig. 8.4 Measured Machine Stator Back EMF for Different Levels of Field Excitation Current.

copper can damper, i.e. the whole rotor winding is inserted into a copper cylindrical can as shown in figure . As highlighted in the earlier discussions, the machine commutating inductance considerably affects the rate at which the stator phase current can commutate from one electronic commutator phase arm to another. This has a direct impact on the current that can be force commutated by the power semiconductors of the electronic commutator. It also has a direct impact on the machine power output due to its influence on the commutation overlap angle. The smaller the overlap angle, the higher the power output since the machine can be operated at a much higher values of commutator firing angles. Additionally, the higher the commutating inductance, the higher the energy per commutation that has to be either dissipated as heat or recovered using additional energy recovery circuits. This has a direct impact on the design, size and cost of the snubber and clamp circuits.

Search coils were built into the stator windings of this prototype machine to enable measurements of machine parameters, such as commutating inductance, armature

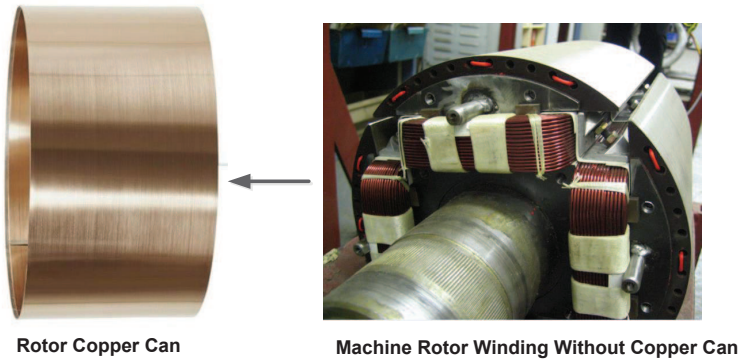

Fig. 8.5 Machine Rotor Winding and Rotor Copper Can Damper Winding.

reaction effects and machine flux. In this machine, measurements were taken before and after the rotor copper can damper winding was inserted to evaluate its impact on reducing the machine commutating inductance. The rotor copper can acts to prevent stator flux penetration into the rotor circuit at high frequencies. The thickness of the rotor copper can was chosen to ensure that the rotor copper can acts at high rates of change of stator current during stator current commutations, where the rotor copper can skin depth becomes fully developed. The rotor copper can thickness was chosen to be 2mm, which corresponds to copper skin depth at 1kHz.

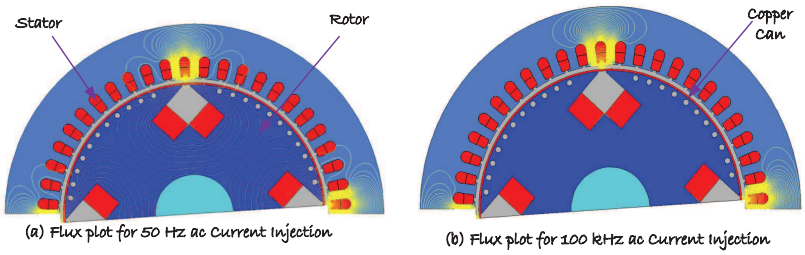

Fig. 8.6 Finite Element Model Flux Plots for ac Injection at 60 Hz and 100 kHz.

The effectiveness of the rotor copper can damper can be easily visualised in Figure 8.6 which shows Finite Element Model (FEM) simulation results when current is injected at 60 Hz and 100kHz in two phase coils which share the same slot with no current in field winding and in the rest of the stator phase coils. The figure show that at 60Hz, the stator flux can still penetrate the rotor because the skin depth of copper at 60Hz is about 8.5 mm. It also shows that at 100kHz the current is confined to the

copper can because the penetration depth in copper is very small and less than the copper can thickness of 2mm.

Figure 8.7 shows the measured machine commutating inductance variation with frequency, with and without the rotor copper can when an ac current was injected in two stator phases that share the same slot. Its clear that at low frequencies, the skin is not fully developed in the rotor can and flux can still penetrate the rotor. At high frequency where the skin depth has fully developed the rotor copper can operates in an inductance limited case where it becomes independent of frequency. It can be seen that at high frequencies, which corresponds to the high rate of change of stator current under forced commutation, the rotor copper can damper winding effectively reduces the commutating inductance from 130 μH to 32 μH.

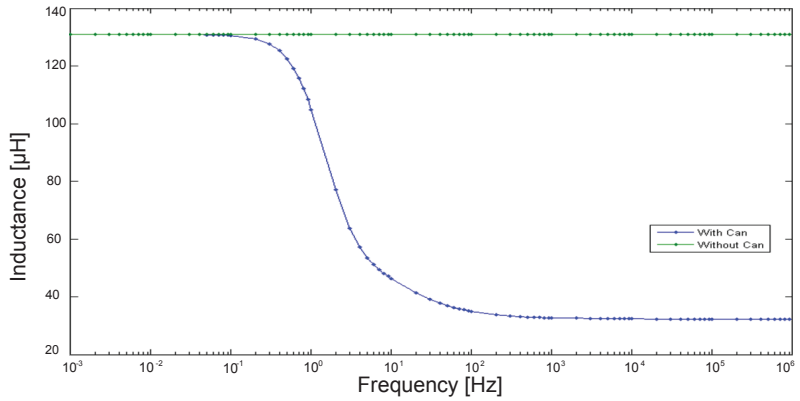

Fig. 8.7 Machine Commutating Inductance Variation with Stator Excitation Frequency with and without Rotor Copper Can

The load drive used for this test rig has the following rating data.

1. Load Drive
    - Machine rated Power = 150 kW
    - Machine stator phase number = 3 $phases$
    - Machine rated stator frequency = 60 Hz
    - Machine type = $Induction \quad machine$
    - Load Converter = $Regenerative \quad active \quad front \quad end \quad drive$

8.4.2 Electronic Commutator Power Electronics

The two level electronic commutator circuit described in chapter 3 was implemented for this 24 phase topology prototype test drive. The electronic commutator circuit comprised of 48 Gate Turn Off (GTO) Thyristor devices with unit gain turn off capability, 48 clamp circuit diodes, 48 GTO gate cards and 2 clamp capacitors. The electronic commutator power semiconductor stacks were assembled as submodules. Figure 8.8 shows the circuit arrangement, a 3D representation and practical implementation of the electronic commutator stack sub assembly. The Electronic commutator GTO stacks were cooled using de-ionised water cooling. The electronic commutator stacks were assembled in a cubicle that was separate from the machine housing and connected to the machine via copper cables as shown in figure 8.9.

Compared to conventional 3 phase topologies at low power ratings, the device utilisation factor is poor. However this machine is aimed at high power applications where conventional machines will require similar device count owing to the increased per phase VA rating required on conventional 3 phase voltage & current source topologies. At these high power levels, conventional 3 phase topologies will require series or parallel device connection which brings with it issues in terms of dynamic and transient voltage and current sharing. This problem is completely eliminated in this topology owing to the reduction in per phase VA rating that comes with increased machine phase number.

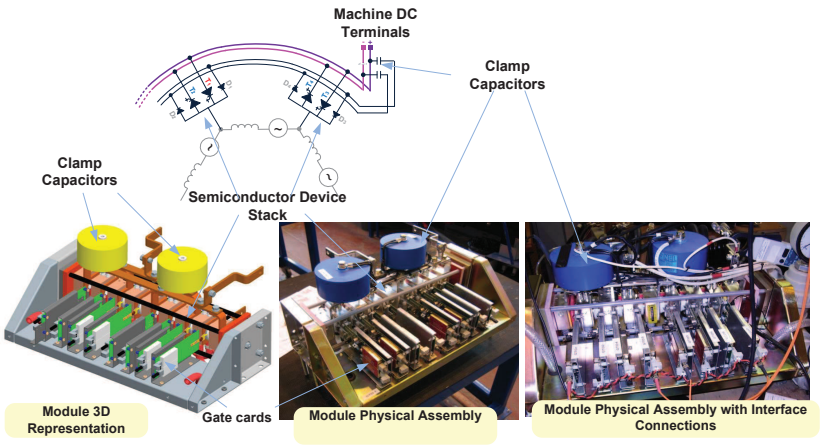

Fig. 8.8 Electronic Commutator Power Electronic Sub Modules Implementation

1. Electronic Commutator Rating:

- Commutator phase number = 24 *phases*
- Rated dc link voltage = 500 Vdc
- Rated Commutator phase current = 300 $Apeak$
- Rated commutator device switching frequency = 60 Hz

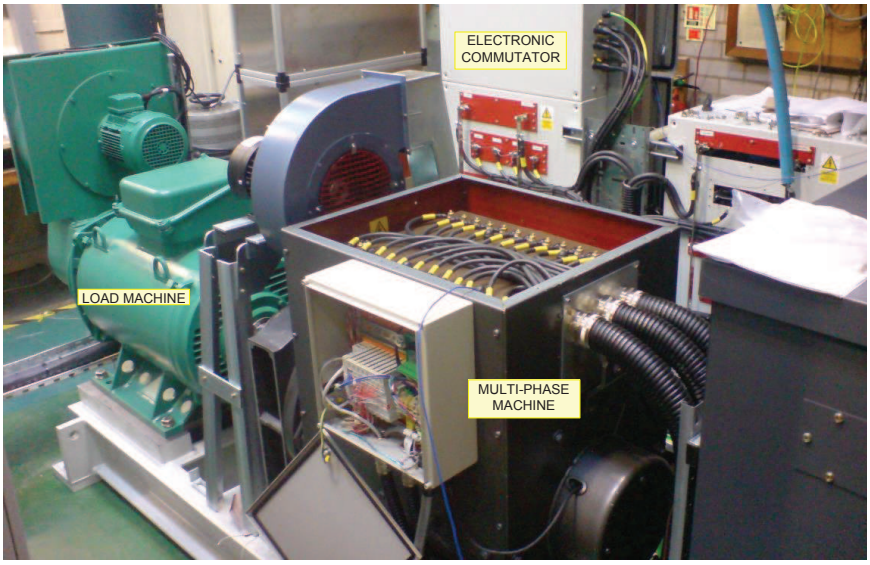

Fig. 8.9 150 kW Laboratory Test Drive for 24 Phase Machine Concept Validation

The 24 phase machine electronic commutator was connected to a regenerative active front end current source rectifier via a 3mH dc link inductor as depicted in figure 8.1. Figure 8.9 shows a picture of the 150kW laboratory test drive used to validate the 24 phase machine and converter topology. As highlighted earlier, no attempt to combine the power electronics with the machine was made in this laboratory drive, it was purely for topology concept operation validation. This experimental prototype laboratory drive was used for the experimental results on even numbered multiphase drive presented in the following chapter.

8.5 Odd Stator Phase Number Test Rig

In addition to validating the same topology features as in the first even numbered laboratory test drive above, the second laboratory prototype drive was designed to investigate and validate two key objectives of this multiphase electronically commutated machine concept. Firstly, the machine rating was selected to enable the concept of machine and converter integration into a single unit to be explored and characterised. Secondly,

having investigated the topology with even number of stator phases, the machine was designed with an odd number of stator phases. The key questions with an odd number of stator phases topology which needed practical validation were, to establish whether the machine will result in a net circulating current in the machine polygonal winding, and also to explore suitable electronic commutator control strategies that would enable correct operation of this odd numbered machine. So this prototype drive was designed to improve the understanding of all aspects of topology design such as; control, power electronics, machine and integration including cooling. Details of the odd number multiphase drive under test and its load drive are summarized in the following sections.

8.5.1 15 Phase Machine

The prototype machine comprised of an odd number of stator phases and a wound rotor field excitation winding. All the stator phase winding functions are phase displaced equally by $\frac{2\pi}{15}$ radians (electrical) and connected to form a complete polygonal winding. Unlike the even numbered machine used in the first prototype machine, simple fully pitched stator phase winding cannot be employed as this would result in undesirable net circulating currents in the machine stator polygonal winding during machine operation. To prevent a net circulating current in the polygon, the machine winding function should be such that the induced phase voltage (machine back emf) of each phase does not contain the 15^{th} voltage harmonic. In this machine, this was achieved by employing short pitched coils and connecting two short pitched coils in series such that the resultant phase winding function does not have any 15^{th} voltage harmonics. To minimize cost, an already existing machine was used for this work. The stator was stripped and rewound to give 15 stator phase windings connected in series to form a single polygon stator winding. Owing to the asymmetry with an odd number of stator phases, the stator phase windings were short pitched to give a winding function that results in suppression of a net circulating current in the stator polygon. The existing rotor and field excitation winding design of the original machine was retained unchanged. The power rating of the machine was chosen to be sufficiently high to enable the power electronics integration of the machine and power electronics to be explored. The machine was designed to be a low speed machine to explore potential

challenges in low speed machine applications such as direct drive wind applications, the machine rating data is summarized below;

1. Machine:
    - Machine rated Power = 450 kW
    - Machine stator phase number = 15 $phases$
    - Machine rated stator frequency = 6.6 Hz
    - Machine rotor type = 4 $saliant \quad pole, \quad wound \quad rotor$
    - Machine rated field current = 273 A
    - Machine Commutating Inductance = 1.86 mH
    - Machine rated phase voltage = 127 $V \quad rms$

Figure 8.10 shows the 15 phase prototype machine used for this concept validation.

Fig. 8.10 15 Phase Prototype Machine

8.5.2 Electronic Commutator Power Electronics

The electronic commutator topology already described for odd numbered multiphase machine was implemented for this 15 phase machine. One of the key implementation features of this commutator practical design was to enable integration of the electronic commutator power electronic circuit within the machine housing. As alluded to earlier,

electromechanical integration of power electronics into the machine housing poses some challenges.

Firstly, the electronic commutator will require robust power electronic electronic components and auxiliary control circuit components that are capable of withstanding the harsh environments that can exist in the machine housing. The thermal demands of power electronic converters and electrical machines vary considerably due to the large heat flux of the power electronics compared to the machine.

Additionally, insulation coordination has to be carefully considered to ensure sufficient voltage creepage and clearance distances between the power electronics components and the machine phase windings. This requirement often goes against compact packaging designs particularly at high voltages where higher creepage and clearance distances are required to avoid insulation failures and flashovers.

The electronic commutator power electronics design implementation sought to address the thermal management and insulation coordination issues in the electromechanical packaging design of the commutator power electronics modules to enable integration into the harsh machine housing environment through the choice of cooling fluid and choice of power semiconductor devices and gating electronics components.

Power Electronics Dielectric Liquid Cooling

To facilitate sufficient insulation coordination in the converter power circuit, voltage creepage and clearance distance have to be respected and these depend on the dielectric strength of the medium in which the converter power electronics is housed. In comparison to air, liquid dielectric cooling requires very small creepage and clearance distances owing to the high dielectric strength of the liquid compared to air. As a result of the reduced creepage and clearance distance, compact power electronics converter footprints can be realised thereby facilitating machine and converter integration.

Liquid cooling has been chosen for the power electronics owing to its higher heat transfer coefficient compared to air-cooling. The cooling liquid used was chosen to fulfil the following constraints; (a)that the liquid is non-flammable, (b) non-toxic, (c) economical, (d) with a freezing point less than (-40^0C), (e) be compatible with various components of the power electronic circuit and cooling system that include

metals, polymers, and ceramics. Additionally, the coolant must possess excellent thermophysical properties, i.e. low viscosity, high specific heat and thermal conductivity. A liquid dielectric coolant was chosen to improve thermal management and reduce voltage creepage and clearance distances in order to reduce the overall power electronics footprint in comparison to conventional water cooled power electronics [218].

A synthetic ester oil, Midel 7131 was chosen as the dielectric cooling fluid for the electronic commutator power electronics. Midel 7131 is a robust, high performance dielectric fluid that delivers long term stability, even when exposed to extreme variations in temperature and high overloads. In addition, its excellent moisture tolerance and oxygen stability give it a considerable advantage over other dielectric fluid options such as mineral oil and natural esters [219]. One of the primary benefits of using Midel 7131 is its ability to operate reliably at high temperatures over a sustained period of time. This in turn allows for more compact power electronic designs, and can yield considerable space savings that satisfy both design thermal, insulation coordination and budget constraints. Other qualities that set it apart from the alternatives include; very low pour point (-60^0C), greater moisture tolerance than mineral oil, self-healing and no sludge formation, unlike mineral oil. Table 8.1 gives a summary of Midel 7131 properties compared to conventional mineral oil.

Table 8.1 Midel 7131 properties compared to Mineral Oil

	Midel 7131	**Mineral Oil**
Fully Biodegradable	Yes	No
Breakdown Voltage kV	> 75	> 70
Moisture saturation ppm	2700	55
Viscosity at 40^0C	29	12
Density at 20^0C	0.97	0.88
Expansion Coefficient	0.00075	0.00075
Permittivity	3.2	2.2
Pour Point ^0C	-60	-50
High Temperature	Excellent	Pour
Fire Safety Class	K3	O1

Un-encapsulated Whole Wafer Power Electronic Device

Standard reverse blocking GCTs wafers were selected as the preferred switching device because they can provide adequate performance at the low switching frequencies that would be used in the machine topologies presented in this work, and they presented a relatively low commercial risk. The electronic commutator power electronics stacks were packaged in hermetically sealed containers to provide isolation and shield the sensitive power electronics from the harsh machine environmental conditions. The hermetically sealed stacks were cooled with synthetic Midel 7131 oil which was also utilised as a liquid dielectric to reduce voltage creepage and clearance distances and provide high voltage isolation in a small footprint in comparison to conventional air insulated power electronic device stack arrangements. To enhance the thermal management of the electronic commutator stack assembly, unencapsulated unpackaged alloyed Reverse Blocking Gate Commutated Thyristors (RB-GCT) with unity gain turn off capability were chosen as the main semiconductor devices to achieve high power density within a sealed stack enclosure. The use of unpackaged alloyed GCT devices is probably the most unconventional attribute employed in the electronic commutator GCT stack arrangement. In this implementation, the GCTs have no outer ceramic housing or module case. In addition to improved thermal performance, this approach lowers the cost of the GCT substantially and yields shorter stacks thereby facilitating compact designs. In this case Midel 7131 is acting as a dielectric and a coolant.

Figure 8.11 shows the components of conventional GCT packaging that were discarded in the implementation when unencapsulated raw wafer GCT devices are used. Its clear that this approach reduces both cost and footprint. Ensuring Power Electronics component compatibility with the liquid dielectric coolant was a major concern, this restricted the choice of unpackaged passivated GCT devices.

1. Electronic Commutator Rating:
    - Commutator phase number = 15 $phases$
    - Rated dc link voltage = 1500 Vdc
    - Rated Commutator phase current = 400 $Apeak$
    - Rated commutator device switching frequency = 6.6 Hz

- Gate Commutated Thyristors = Bare wafers, VDRM:1100 V, ITCM: 600 A (3 devices in series were used)
- Clamp Diodes = bare wafers, VRRM: 4500 V, IT(AV) = 430 A

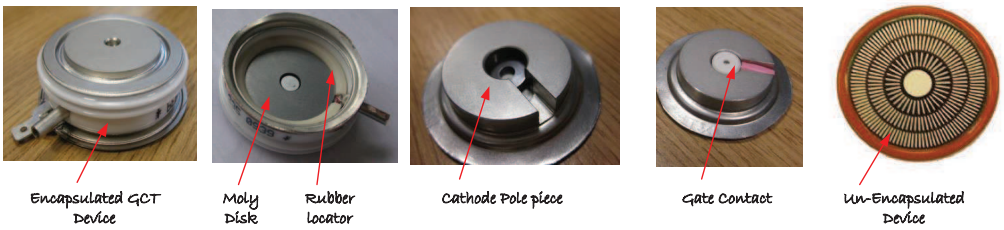

Fig. 8.11 Components of the Encapsulated GCT Semiconductor Device

Figure 8.12 shows the arrangement used with the un-encapsulated GCT devices for immersion in a liquid dielectric Midel 7131 coolant for better thermal management.

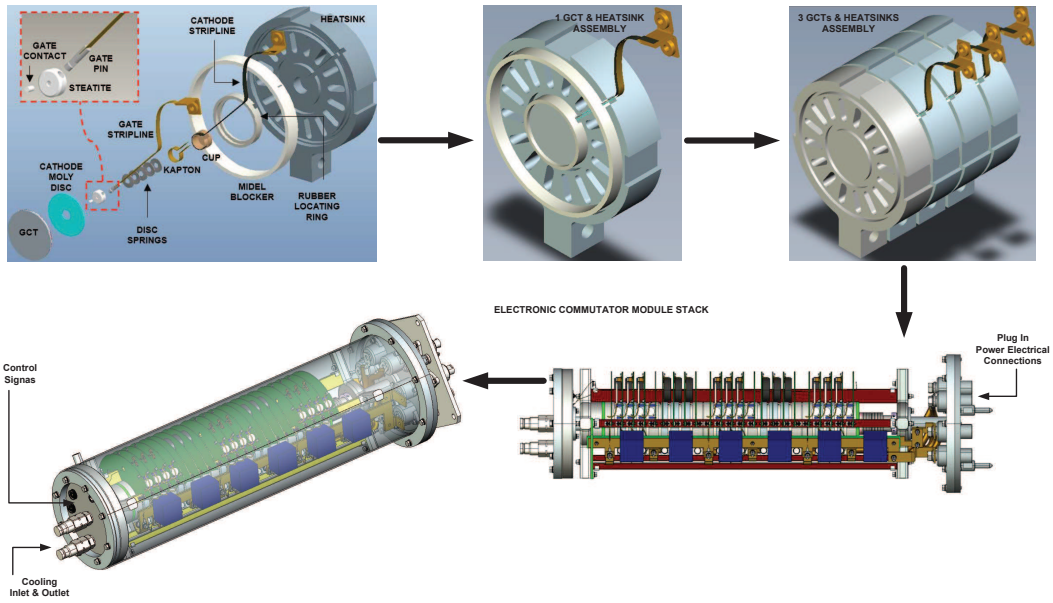

Fig. 8.12 Components of the Un-encapsulated GCT Semiconductor Device Packaging Used

Figure 8.13 shows an illustration of the electronic commutator modules mounted as plug in modules on the machine stator frame.

Figure 8.14 shows the cooling circuit used in the practical implementation of the electronic commutator thermal management.

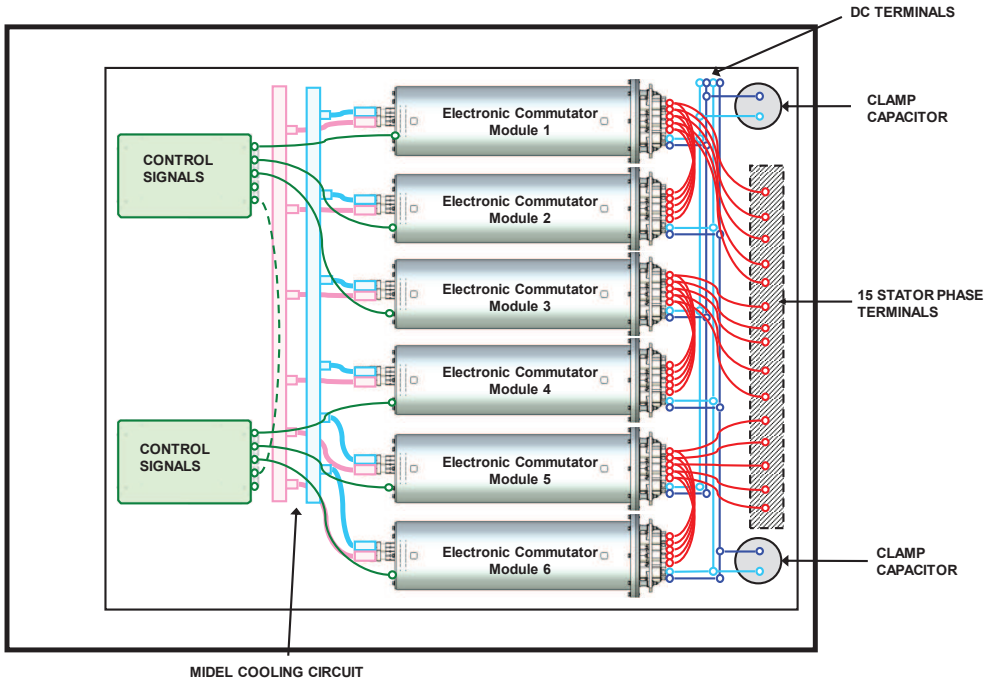

Fig. 8.13 Concept Of Electronic Commutator Plug In Modules Mounted on Machine Stator Frame

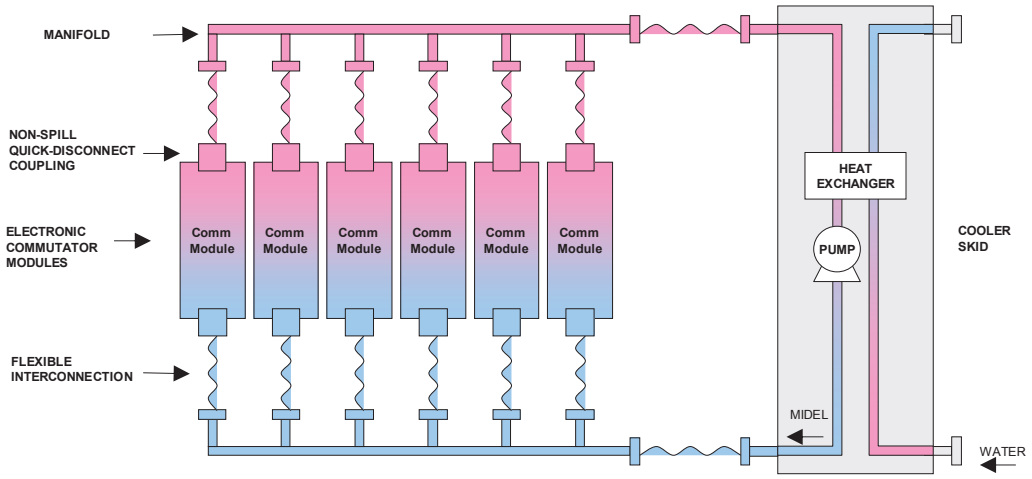

Fig. 8.14 Midel Cooling Circuit for The Power Electronic Commutator Modules

Figure 8.15 shows the practical implementation plug in hermetically sealed Midel cooled electronic commutator power electronics modules integrated into the machine stator frame housing.

As highlighted earlier, compatibility of the electronic commutator components with Midel was a concern. A list of materials compatible with midel is given in [219],

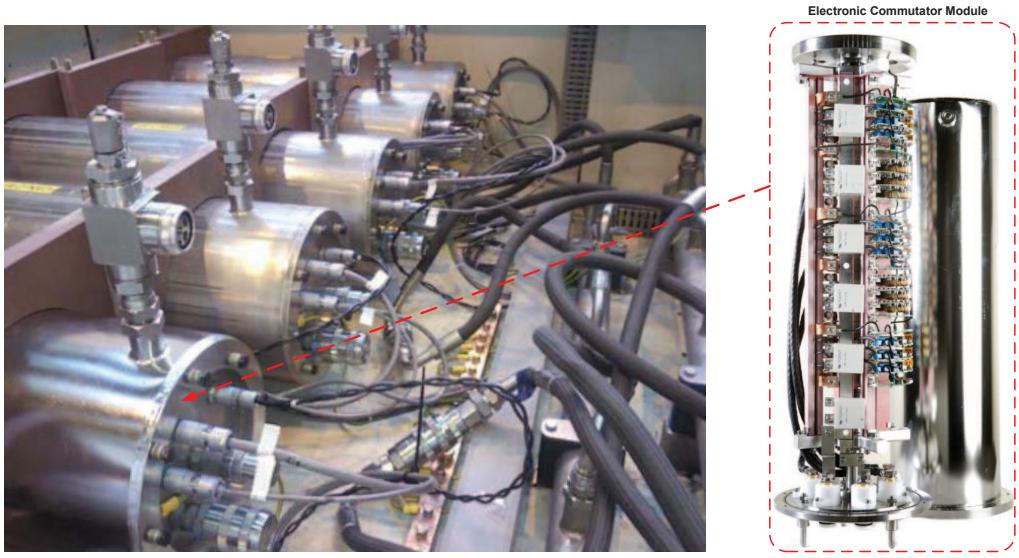

Fig. 8.15 Electronic Commutator Power Electronic Modules integrated as Plug in Modules in Stator Frame Housing

however this list is not exhaustive and does not cover some of the components and materials needed for direct liquid cooled power electronics using Midel. To investigate this further, a complete electronic commutator power electronic module assembly with its associated gating electronics was subjected to tests to characterise its performance over a period of time. Performance measurements including voltage withstand and functional tests were carried out on the power electronic components before immersion into Midel. Tests were conducted over a period of more that one year to assess the degradation in performance if any, of the power electronic components. The results confirmed that all the chosen power electronic components and gating electronics components did not degrade in performance in Midel. Figure 8.16 shows the Electronic commutator components subjected to the long term midel compatibility test. Tests were also carried out on the modules after being subjected to prolonged operation at rated current in Midel and the results showed similar performance and confirmed components compatibility with midel. Some of the materials used in this prototype design that were found to be compatible with midel include: (a) potting compounds such as; Silicone, epoxy, polyurethane, (b) ceramic materials for electronics packaging such as, Alumina (Al_2O_3), Silica (SiO_2), Porcelain & Printed Circuit Board (PCB) mounted capacitor dielectrics, (c) Metals such as Copper, Aluminium, Zinc plated steel, Stainless steel, lead-free solders, (d) Silicon based Semiconductors, (e) Electronics

magnetic material such as Zinc Ferrites, (f) glass epoxy PCB material & Opto-isolator materials such as (SiO_2). However, if opto-couplers are used, care should be taken to ensure the opto-coupler' optical channel are fully closed to prevent ingress of midel as this would adversely alter the refractive index and impede light propagation between the two galvanically isolated sections of the opto-couplers.

Its envisaged that the GCT based electronic commutator design topology will lead to reliable electronic commutators with similar or even better reliability compared to IGBT device type based implementations. A review of reliability of GCT gating electronics compared to conventional IGBT gate cards highlighted that they are more reliable in comparison to the their IGBT counterparts [220–223].

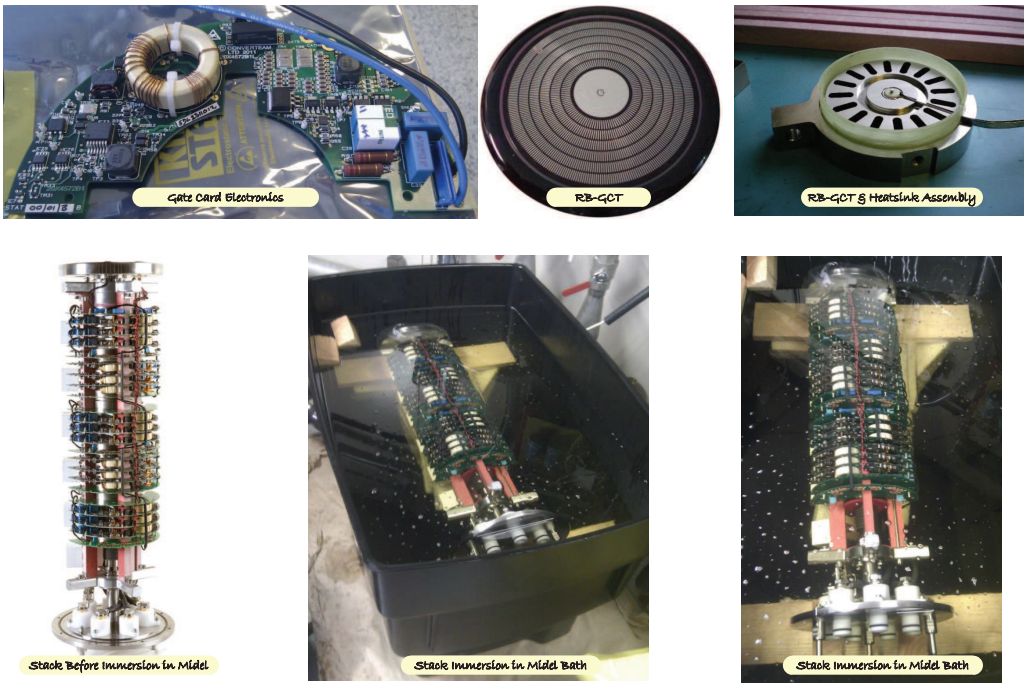

Fig. 8.16 Electronic Commutator Power Electronic Components Midel Long Term Compatibility Test

The benefits of using Midel as a liquid dielectric coolant have been outlined above. In comparison to water cooled stacks, the drawback of using Midel is reduced heatsink performance since Midel has half the specific heat capacity of water, and is much more viscous, leading to more coolant pump power. Alternatively, air-cooling systems may yield simpler designs with no pump, no de-ioniser, no heat exchanger etc. However, air cooled systems carries have significant disadvantages. For example, large quantities

of air can give rise to real problems of pollution on the creepage and clearance paths, requiring bigger distances between conductors hence large footprints. Additionally, in dirty, dusty or salt-laden atmospheres, air cooling requires filters, which can compromise the cooling capacity, and make arc containment more difficult. The use of hermetically sealed Midel cooled stack arrangement mitigates these disadvantages and has been adopted for cooling the electronic commutator devices.

8.6 Control System

To enable validation and characterisation tests to be performed on the multiphase electronically commutated machine and converter, suitable control strategies had to be designed and implemented in suitable control hardware. The control strategy form this machine discussed in earlier chapters was implemented and experimentally validated. Figure 8.17 shows the overall control hardware and how its interfaced to the machine and electronic commutator power electronics. The control hardware comprise of the

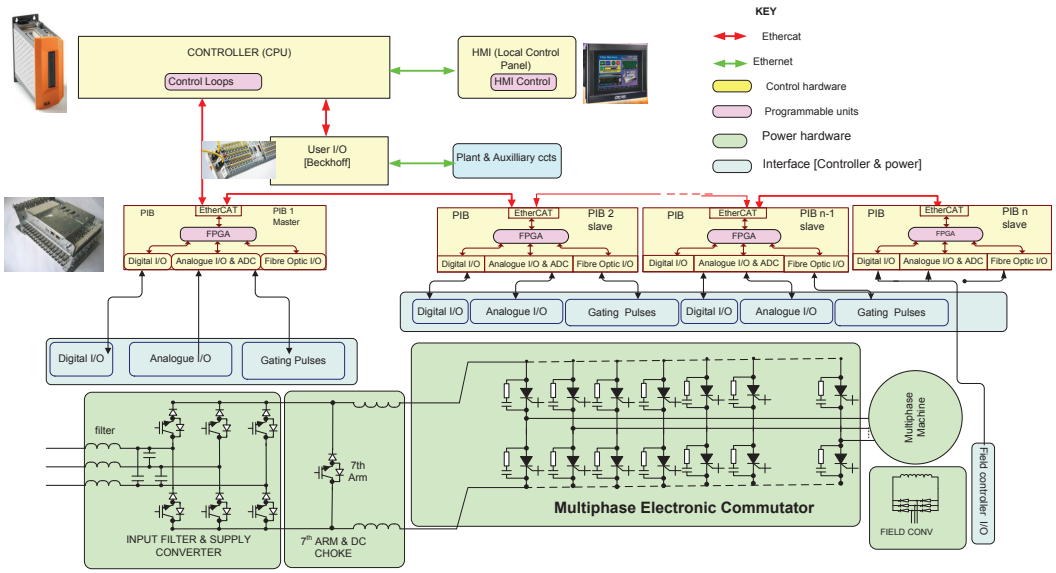

Fig. 8.17 Schematic Showing Control Hardware and its Interfaces to the Power Electronics Hardware

following;

Central Processing Unit (CPU) The CPU used is an off the shelf industrial controller from B&R [224]. All the formulated machine and converter slow and fast

control loops were implemented in this CPU running with a scan time of $200\mu s$. The CPU also interfaces to control panels and programming computers.

Power Interface Board (PIB) The PIB contains the Field Programmable Gate Array (FPGA)use to generate all the gating signals for the power electronic devices from the firing event commands computed in the CPU. The PIB handles the interface between the CPU and the power electronics hardware. It also provides the galvanic isolation between the power electronics hardware devices thanks to the fibre optic interface between the PIB and the Power electronics. All the feedback signals analogue to digital conversion is also performed by the PIB control board. Data transfer between the CPU and the PIB units is via a proprietory ethernet protocol specially formulated for transmission of control data in real time.

8.6.1 Overall Control System

The various control loops discussed earlier were implemented in the above control hardware. Figure 8.18 shows the overall control scheme implementation for the multiphase electronic commutator drive. The various control loops implement the control strategy discussed in the control chapters presented earlier and will not be repeated here, only the implementation aspects will be discussed and highlighted. The key areas implementation aspects of the control scheme that will be discussed will focus on the control and implementation aspects of the electronic commutator and the network bridge current source rectifier for this topology.

8.6.2 Electronic Commutator Control Implementation

One of they aims of the validation work was to enable demonstration that the proposed control strategy for both odd and even numbered multiphase machine electronic commutators can be accurately controlled to mimic the operational characteristics of conventional mechanical commutators of dc machines. The main control functions of the electronic commutator include:

(a) Ensuring perfect electronic commutator phase devices firing and synchronisation to the machine phase stator voltage vector.

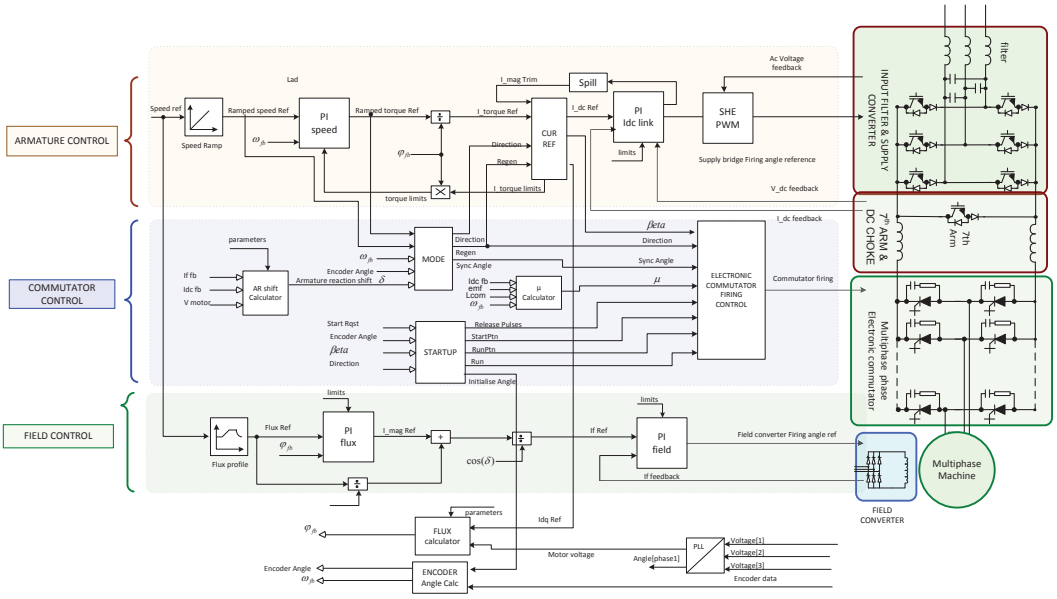

Fig. 8.18 Schematic of the Overall Multiphase Electronically Commutated Machine Implementation Showing all Control Loops

(b) To ensure safe stator phase current commutation by the electronic commutator.

(c) To control and facilitate electronic commutator operation in three commutation modes; natural commutation, forced commutation and hybrid commutation.

(d) To control the machine operating power factor Power factor and operation of machine in both motoring and generating quadrants.

(e) To ensure safe shutdown of the machine electronic commutator.

All these control features were accounted for in the implementation of the electronic commutator control strategy for both even and odd numbered multiphase machine prototypes.

Electronic Commutator Control Input Variables

Synchronisation Angle θ: This is the synchronisation phase reference angle (in radians) for the commutator firing module. The phase reference is derived from either the encoder signal and load angle or calculated from the stator voltage feedback signals. It represents the position of the stator flux vector relative to phase 1 axis of the stator.

Positive direction for angle ramping from zero to 2π and negative direction for angle ramping from 2π to zero.

Firing Angle Reference α: It is the firing angle reference (in radians) used to determine when firing pattern changes are to occur relative to the synchronisation phase reference. Its equivalent to $(\pi - \beta)$ where β is the firing delay angle. The firing angle reference dictates the commutator operating mode, whether rectifying (generating) or inverting (motoring). The firing angle control was implemented to enable smooth transitions between motoring and generating modes over the entire drive operating range.

Overlap Angle μ: It is the overlap angle (in radians) where the outgoing phase device and incoming phase device are both gated on. The overlap angle is employed in commutators with GCTs to enable safe forced commutations when the dc link current to be commutated is above the maximum gate commutated current limit $(I_{COM_{MAX}})$ for the GCTs. In this case, forced commutation at constant gate commutated current where the out-going GCT turn-off follows a preparatory reduction in anode current by means of a conventional Thyristor naturally commutated. The firing angle reference will be adjusted by the overlap angle (μ) so that when the out-going Thyristor is gated-off (at its geometrical neutral axis), its current will have reduced to $(I_{COM_{MAX}})$.

The overlap angle μ is governed by the machine commutating voltage E and commutating inductance $L - c$. The machine topology presented here will ideally benefit from trapezoidal voltage operation and low commutating reactance. An increase in E/L_c reduces μ. It is desirable to maximise E/L_c, within the limits of power semiconductor switching stresses, because this is expected to improve the machine power factor and output coefficient, whilst reducing the demand for excitation. As alluded to earlier, some applications may require an optimised combination of natural and forced commutation, this machine and commutator topology can tolerate over-commutation without sparking because the semiconductor devices reverse recovery blocks the current reversal that would otherwise be interrupted by brush commutator action. If GCT type devices are employed, under-commutation can be tolerated without sparking, the gate turn off process displaces the sparking. Thus, the ability to vary the

overlap angle μ is paramount and was implemented in the commutator control scheme to enable the above functionality is to be realised.

Electronic Commutator Control Output Variables

The electronic commutator firing control module can produce up to 24 firing command outputs for the FPGA to decode and generate the GCT gating signals in real time. Each of the firing command from the CPU has been structured as sh0wn in table 8.2.

Table 8.2 Electronic Commutator GCT Firing Command Structure

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid	State	Firing Event Time													

Firing Event Time :This is the CPU computed time where the next firing event is to occur in real time. The time is measured by the FPGA in the Power Interface board (PIB) as FPGA ticks. Each FPGA tick represents a resolution of 133.333ns of the real time. In this implementation, the first 14 bits are used for the firing event time. The **State bit** represents the action to be taken when the calculated firing time equals the FPGA tick count, i.e. whether a device is to be turned ON $(state = 1)$ or OFF $(state = 0)$. The **Valid** bit will be used to check whether the firing event command is valid or not (Valid = 1) and (not valid = 0).

Commutator Device Firing Event Calculation The electronic commutator power electronic device switching control has been formulated to mimic the operational characteristics of the conventional mechanically brush commutated dc machines. The electronic commutator power power electronic device firing event calculation determines which device is to be turned ON or OFF and computes the time when the firing event is to occur relative to the PIB FPGA clock counter ticks in real time as highlighted in figure 8.20. The calculation of the firing event time is done by the CPU and is executed every Fast Task Interrupt (FTI) period. The electronic commutator firing event command is then decoded by the PIB FPGA to generate the firing signal to the electronic commutator devices. The explanation below is given in reference o the control hardware illustration in 8.19.

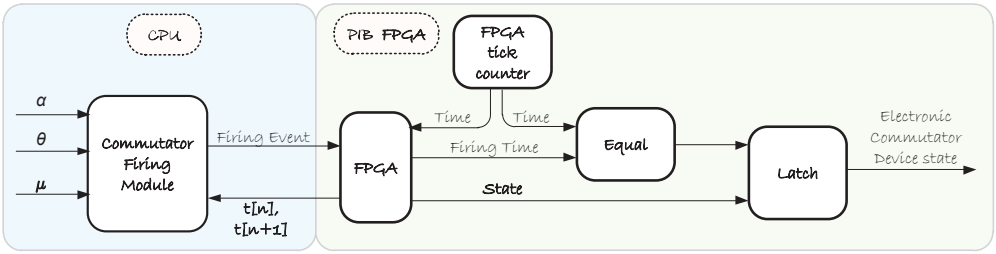

Fig. 8.19 Electronic Commutator Control Hardware Implementation

The following summarises the Electronic commutator firing event calculation for the semiconductor switching devices.

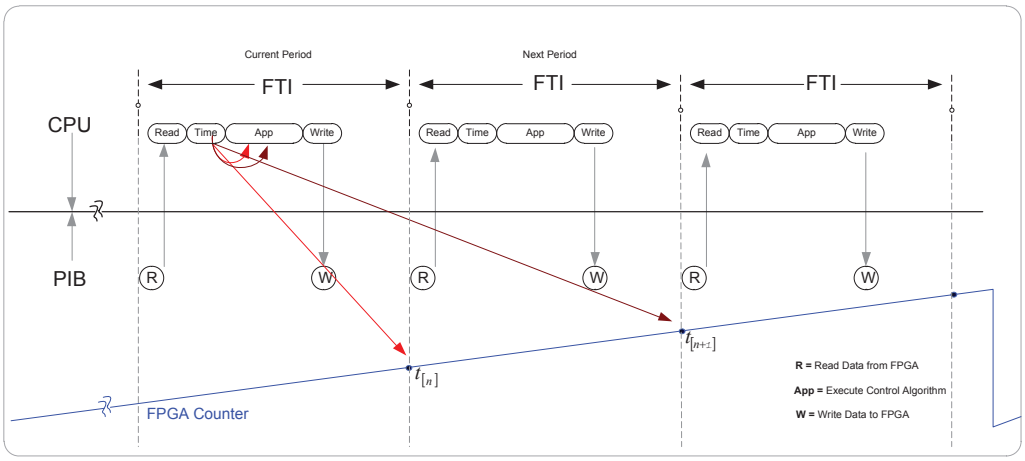

Fig. 8.20 Simplified Schematic Illustrating Timing Between CPU and PIBe

Firstly, the change in the machine stator voltage position angle change since the last CPU Fast Task Interrupt (FTI) is computed as:

$$\theta_{\Delta} = \theta_{[n]} - \theta_{[n-1]} \tag{8.1}$$

where $[n]$ represents current value and $[n-1]$ represents last FTI value of stator voltage position angle θ.

The velocity of the stator voltage vector is computed by; Calculate change in FPGA time to next FTI:

$$\upsilon_{\theta} = \theta_{\Delta}/t_{\Delta} \tag{8.2}$$

where t_{Δ} is the change in FPGA time between FTI events given by;

$$t_{\Delta} = t_{[n+1]} - t_{[n]} \tag{8.3}$$

where $t_{[n+1]}$ represents the end of the next FTI event time value of the PIB FPGA clock time.

Next the angle where the next stator phase commutation event is to occur is computed based on the current stator voltage position angle as;

$$\theta_{np} = k_{np}\theta_{np} + \theta \tag{8.4}$$

where, k_{np} is the next commutator device to be fired and θ_{np} is the angle offset between commutator devices such that $\theta_{np} = (2\pi/N)$ and N is number of stator phases.

The change required in stator voltage vector position from the current position to when the next stator phase commutation event is due to occur is given by;

$$\theta_{\Delta_n} = \theta_{np} - \theta \tag{8.5}$$

Using (8.5) the event time when the next stator phase commutator commutation device is to be turned ON is computed by;

$$t_{on} = \theta_{\Delta_n}/\upsilon_{\theta} \tag{8.6}$$

Next, the FPGA switching event time for (8.6) is calculated relative to the current FPGA FTI real time clock as;

$$t_{event} = t_{[n]} + t_{on} \tag{8.7}$$

Based on the required electronic commutator operating mode i.e. whether its employing forced commutation or natural commutation or a combination of the two, the desired commutation overlap is inserted between the adjacent commutation events. The real time when the commutator phase device that is currently ON is due to be

turned OFF is computed as;

$$t_{event} = t_{[n]} + t_{on} + t_{\mu} \tag{8.8}$$

where $t_{\mu} = \mu / \upsilon_{\theta}$ is the overlap time.

Finally the pattern index for the stator phase commutator device that will be commutated next is computed as;

$$k_{np} = k_{np} \pm 1 \tag{8.9}$$

The pattern index is incremented or decremented depending on the machine rotational direction. The above routine is executed every CPU interrupt and the generated firing commands for electronic commutation are decoded in the FPGA to generate the electronic commutator device switching commands in real time.

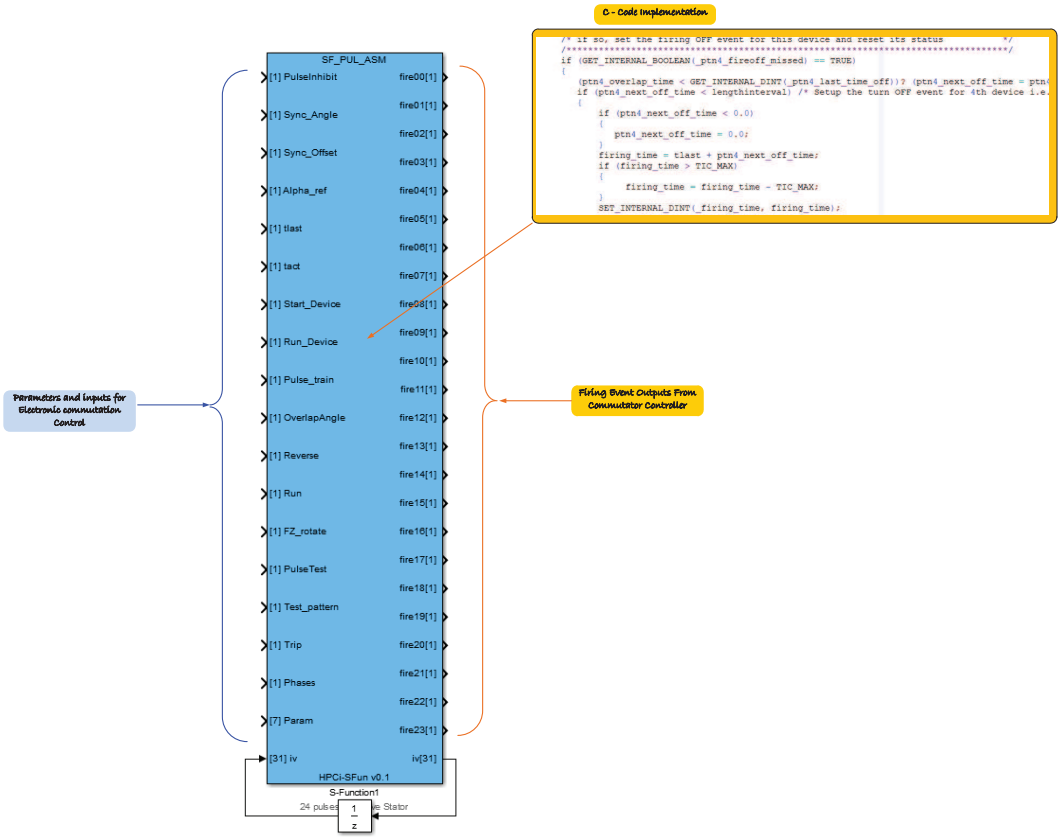

Fig. 8.21 Electronic Commutator Control Module Implementation & Matlab S-Function Implementation

Commutator Device Firing Control The control function for the Electronic commutator was implemented in C-code in the CPU. The same C-source code was used in the Matlab Simulink modelling using portable executable Dynamic Link Library (DLL) files and S-function features of Matlab/Simulink as shown in figure 8.21. This approach facilitated rapid initial validation via simulation as test vectors can readily defined to fully exercise the control source code implementation via simulation before deployment on the hardware platform. Figure 8.22 shows the generated electronic commutator firing commands for a 24 phase electronic commutator when the speed is ramped from zero to 1.0 pu steady state and then reversed to -1.0 pu. As can be seen in this figure, the electronic commutator control scheme is capable of synchronising the machine phase commutation accurately to track the machine stator voltage vector position even through quadrant changes between motoring and generating modes and speed reversals.

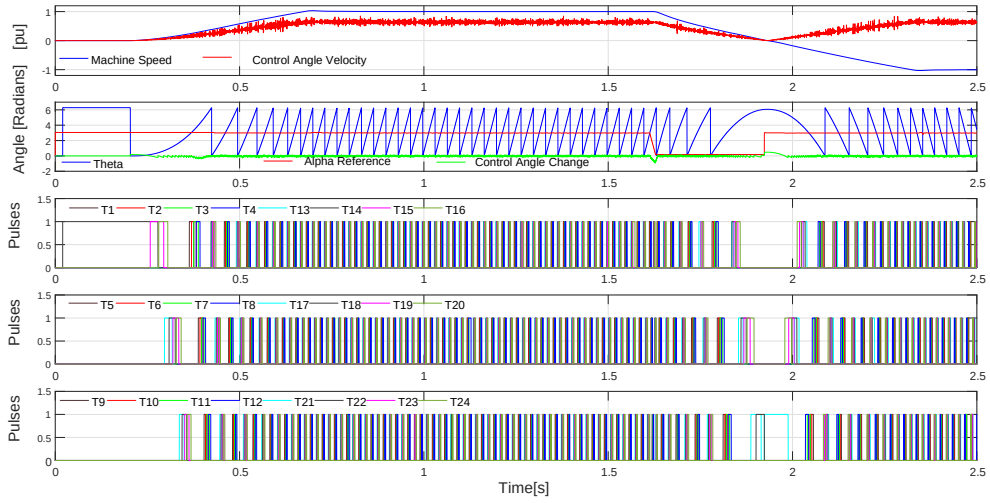

Fig. 8.22 Simulated Electronic Commutator Control Operation for Machine Speed and Quadrant Changes

Figure 8.23 shows a zoom in of figure 8.22 for commutator control during speed reversal.

The firing of the electronic commutator phase power electronic devices is synchronised to the voltage behind reactance of the respective commutating phase. This voltage is dependent on the direction of machine rotation. For example, the switching of commutator switching device T_3 in figure 8.24 is synchronised to the phase voltage

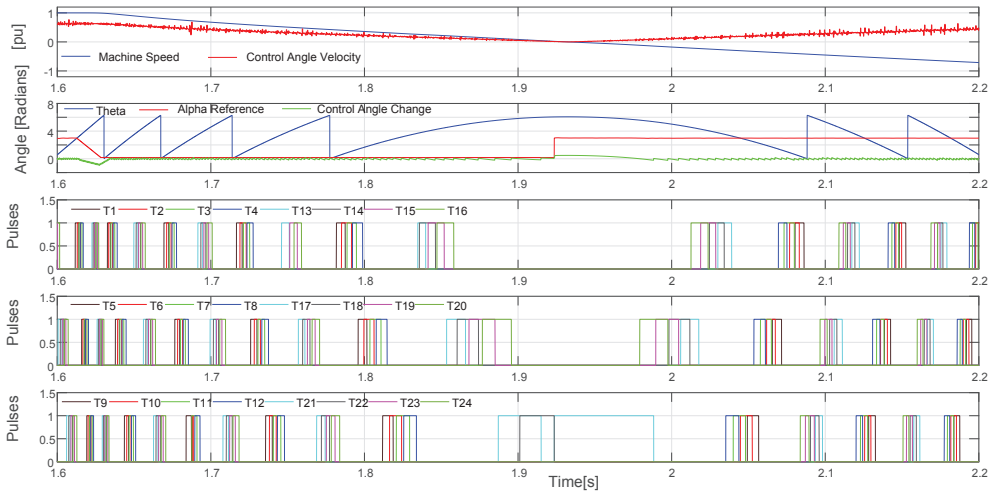

Fig. 8.23 Simulated Electronic Commutator Control Operation for Machine Speed Reversal

V_3 when the machine direction of rotation is clockwise. For anticlockwise machine rotation, the switching of the same device T_3 has to synchronise to the phase voltage V_4.

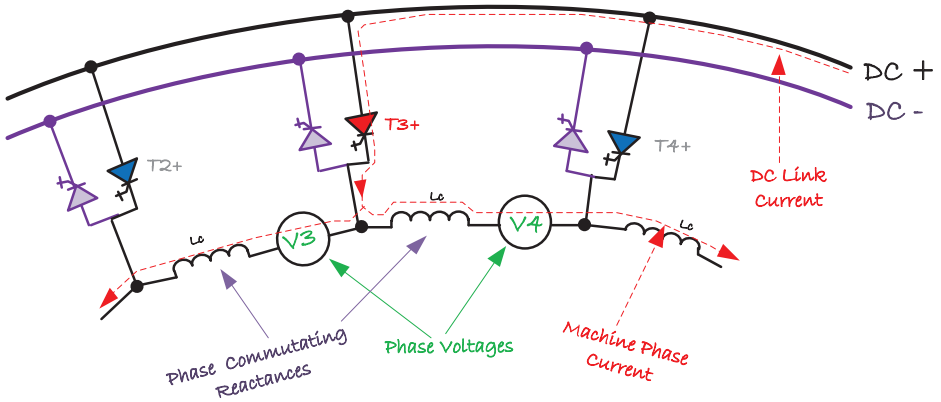

Fig. 8.24 Electronic Commutator Phase Synchronisation

8.6.3 Network Bridge Control Implementation

This section describes the control functionality of the Current Source Rectifier (CSR) used as a regenerative front-end converter for the multiphase electronically commutated

dc machines. This is based on the earlier work reported in [225]. Figure 8.25 shows a schematic diagram of the CSR topology used in the prototype drive. A single CSR converter was used in the 24 phase prototype drive, two series connected CSR converters with interleaved PWM was used in the 15 phase prototype drive. The CSR adopted employed a Selective Harmonic Elimination (SHE) modulation algorithm to eliminate trouble some low order harmonics from the ac grid side and at the same time minimise converter switching losses. Various SHE PWM strategies are widely documented in literature [112, 226, 109, 227, 228, 101], as such, this section will only detail the implementation features of the SHE strategy adopted in this work. IGBTs with series blocking diodes were used in the experimental test rig simply due to availability of these devices, GCT devices are equally applicable for the current source rectifier.

In the SHE modulation scheme adopted, a combination of current chops and short circuit pulses are strategically positioned by the six arm devices of the CSR relative to the fundamental ac phase voltage in such a way that lower order ac harmonics are eliminated selectively in addition to dc link current magnitude modulation. Rather than using two series arms of the CSR to apply the short circuit pulses, the 7th arm is used instead to reduce the conduction losses. The CSR converter switching device labels adopted in figure 8.25 is used in subsequent discussion. As highlighted in the electronic commutator implementation, the same control hardware is used for the control of the CSR. The high bandwidth control algorithms and calculation of the firing events for the CSR power electronic devices has been implemented in the CPU. The acquisition of the digital and analogue inputs/outputs and decoding of the firing events to generate CSR device switching pulses has been implemented in the PIB FPGA, similar to that of the electronic commutator.

SHE PWM Implementation

The SHE modulation with 7 chopping angles has been adopted to control the fundamental component of the CSR line current and to eliminate 5th, 7th, 11th, 13th, 17th & 19th harmonics from the supply line currents. To avoid even harmonics, quarter wave symmetry is employed. To ensure continuity of current in the CSR, the seven chopping

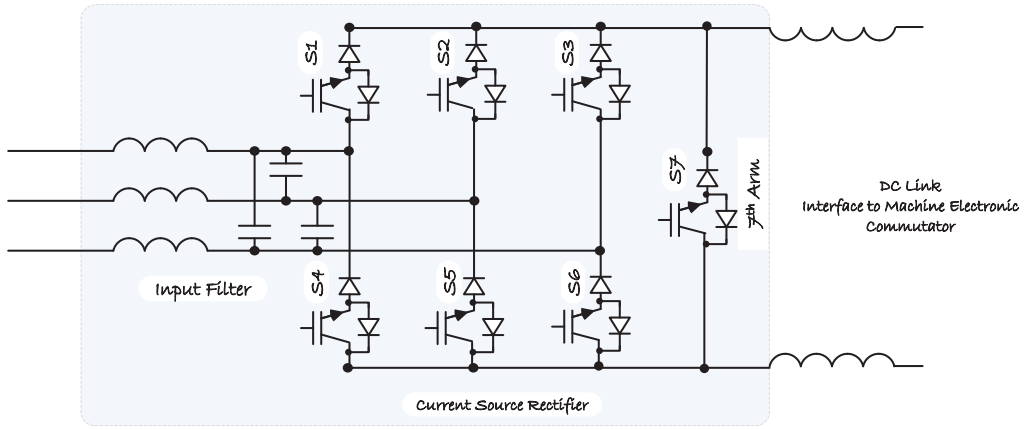

Fig. 8.25 Current Source Rectifier Topology Used In Prototype Drive

angles are calculated between 0 & pi/6 and the waveform before and after pi/6 is an inverse mirror image. This means there is no chopping between pi/3 & 2pi/3 interval for S1, S2 & S3. To generate the 7 chopping angles, a set of non-linear equations (see below) are solved as a function of modulation and harmonics to be eliminated. Similar to the strategy reported in [229], the magnitude of the fundamental CSR line current for the 7 switching angles can be derived and written as:

$$\begin{aligned} m = \frac{4}{\pi}\{&\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_4) - \cos(\alpha_5) + \cos(\alpha_7) - \cos(\frac{\pi}{6}) \\ &+ \cos(\frac{\pi}{3} - \alpha_7) - \cos(\frac{\pi}{3} - \alpha_6) + \cos(\frac{\pi}{3} - \alpha_4) - \cos(\frac{\pi}{3} - \alpha_3) \\ &+ \cos(\frac{\pi}{3} - \alpha_1) - \cos(\frac{\pi}{3} + \alpha_2) + \cos(\frac{\pi}{3} + \alpha_3) \\ &- \cos(\frac{\pi}{3} + \alpha_5) + \cos(\frac{\pi}{3} + \alpha_6)\} \end{aligned} \tag{8.10}$$

where the modulation is given by the ratio of the peak fundamental ac current to the rated dc link current (I_{dc}) as;

$$m = \frac{I_{ac_{peak}}}{I_{dc}} \tag{8.11}$$

The magnitude of the n^{th} harmonic in the ac current is given by;

$$\begin{aligned} I_n = \frac{4}{n\pi}\{&\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_4) - \cos(n\alpha_5) + \cos(n\alpha_7) - \cos(n\frac{n\pi}{6}) \\ &+ \cos(n(\frac{\pi}{3} - \alpha_7)) - \cos(n(\frac{\pi}{3} - \alpha_6)) + \cos(n(\frac{\pi}{3} - \alpha_4)) - \cos(n(\frac{\pi}{3} - \alpha_3)) \\ &+ \cos(n(\frac{\pi}{3} - \alpha_1)) - \cos(n(\frac{\pi}{3} + \alpha_2)) + \cos(n(\frac{\pi}{3} + \alpha_3)) \\ &- \cos(n(\frac{\pi}{3} + \alpha_5)) + \cos(n(\frac{\pi}{3} + \alpha_6)) - \cos(n\frac{\pi}{2})\} \end{aligned} \tag{8.12}$$

To calculate the corresponding chopping angles for controlling the modulation and cancelling the specified ac line harmonics, the desired fundamental component is set to m and the harmonic components are set to zero. This gives a system of nonlinear equations that can be numerically solved offline and implemented as lookup table of chopping angles against modulation index in the control scheme. The complete trajectories for the individual angles as a function of the modulation index m are depicted in figure 8.26 which shows a plot of the variation of the switching angles with modulation.

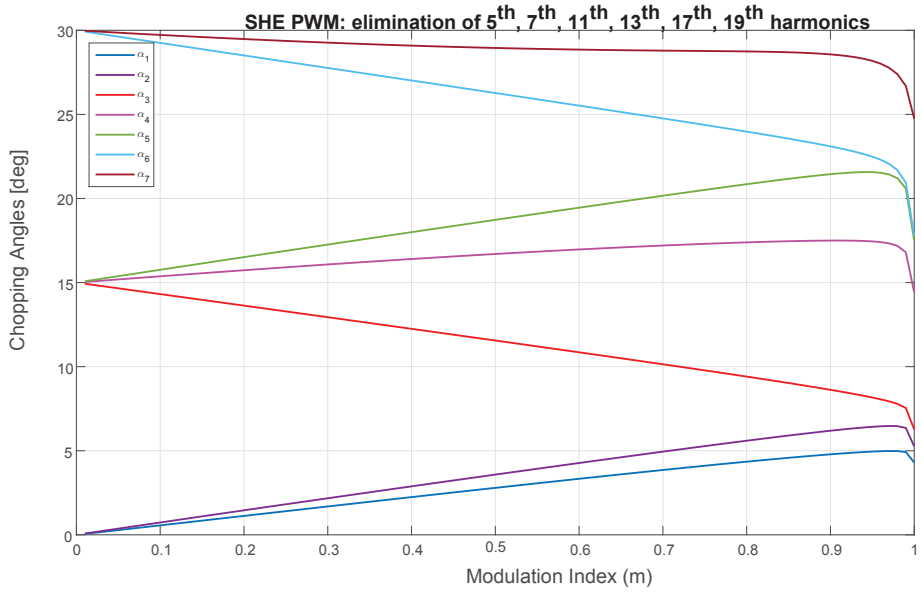

Fig. 8.26 SHE PWM Switching Angles as a Function of Modulation

The chopping angles tend to converge at the extremes of modulation index, i.e. towards $m = 0$ and $m = 1$. This presents a limitation in terms of the practically

achievable modulation index owing to the power electronic switching device minimum on time constraints.

For the control scheme practical implementation, the position of the input ac line current over a fundamental cycle is mapped into one of the six sectors. Each sector representing $\frac{\pi}{3}$ radians. Each of the 6 sectors is subdivided into 16 segments and each segment within a sector is associated with a particular state of the CSR switching devices S_1 to S_7 as highlighted in figure 8.27. The amplitude of each segment is a function of the modulation index, according to the angles stored in the look-up-table. To facilitate implementation of the SHE modulation scheme, the CSR can be viewed as a uni-directional state machine with 97 states, each state representing a segment within a sector. A state machine as depicted in figure 8.27 was implemented in the FPGA to generate the switching devices gating signals which map the desired position ac line current to the switch states in real time. A table of the CSR switch state for 97 segments is given in appendix C.1. For each switch S_1 to S_7; 0 implies an open switch & 1 implies a closed switch. An extra state (not in any of the 6 segments below) where the S_1 to S_6 switches are open and S_7 (7^{th} arm switch) is closed will be used as the trip state/initial state to provide a free wheeling path for the dc link inductor current. Figure 8.28 depicts the partitioning of the control scheme implementation between the CPU and the FPGA, similar to the scheme adopted for the electronic commutator implementation.

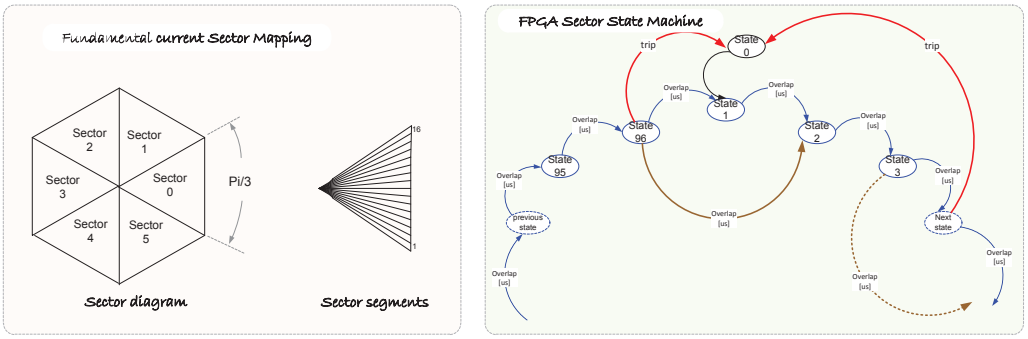

Fig. 8.27 SHE PWM Converter Switching Sectors and FPGA Sector State Machine

For each switching event that occurs in an FTI period, the SHE control algorithm in the CPU generates two event commands to the FPGA.The first command contains the event time, i.e. the future FPGA clock time when the firing event is to occur. The

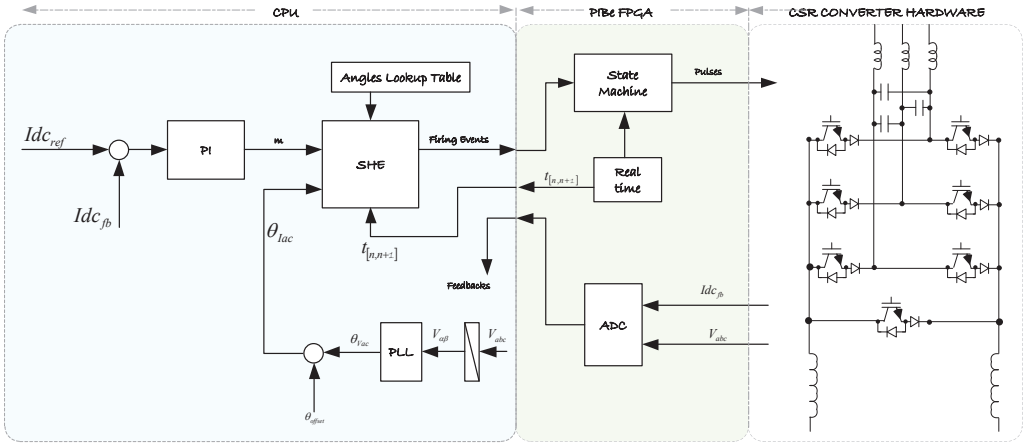

Fig. 8.28 SHE PWM Control Scheme Implementation Partitioning

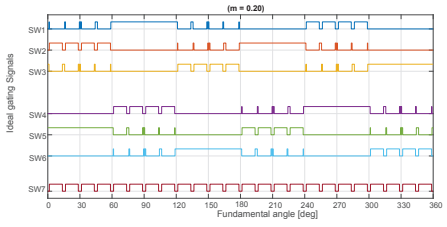

Fig. 8.29 SHE PWM CSR Switching Devices Gating Waveforms for a Fundamental Cycle at 20% Modulation

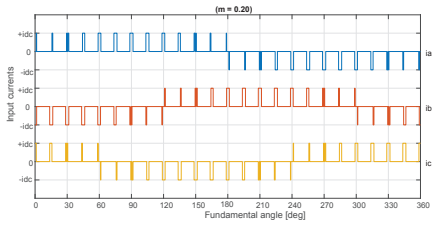

Fig. 8.30 SHE PWM CSR ac Line Currents Waveforms for a Fundamental Cycle at 20% Modulation

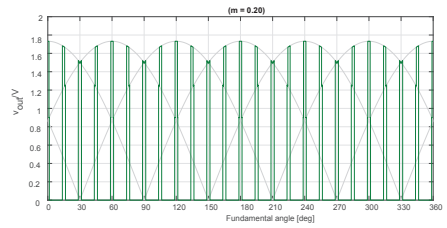

Fig. 8.31 SHE PWM CSR Output DC voltage Waveforms for a Fundamental Cycle at 20% Modulation

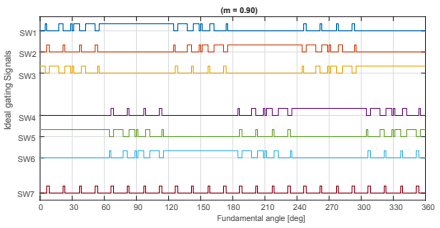

Fig. 8.32 SHE PWM CSR Switching Devices Gating Waveforms for a Fundamental Cycle at 90% Modulation

second command contains the state number which the FPGA state machine should go to at the desired computed event time. The calculation of the event time is similar to that described for the electronic commutator and will not be repeated here. The FPGA decodes the two words and moves the state machine into the desired state in real time relative to the fundamental ac voltage to give the CSR gating pulses. Figure 8.29, figure 8.30, figure 8.31, figure 8.32, figure 8.33 and figure 8.34 show the simulated

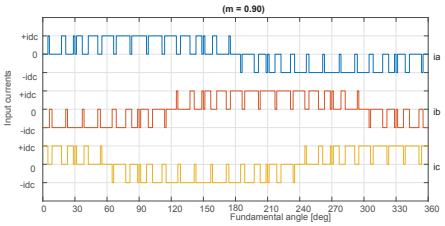

Fig. 8.33 SHE PWM CSR ac Line Currents Waveforms for a Fundamental Cycle at 90% Modulation

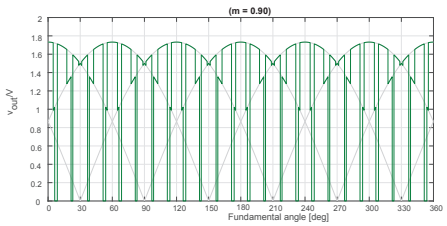

Fig. 8.34 SHE PWM CSR Output DC voltage Waveforms for a Fundamental Cycle at 90% Modulation

control scheme SHE PWM CSR gating signals for devices S_1 to S_7 , input line currents and output dc link voltage for 20%and also 90% modulation over a fundamental cycle.

8.7 Discussion

The machine and power hardware described in this chapter together with the associated control schemes were implemented on the two laboratory test drives. The two laboratory test drives were used for the final validation of the prototype concepts discussed earlier. The same source code developed for the machine & converter topologies control schemes was used in both the simulation modelling work and also in the control hardware of the prototype drives. The experimental work was also used to validate the simulation models developed as part of this work. The validation of the simulation models will enable optimisation of the electronic commutator and network converter power electronics designs. The following chapter presents some of the experimental and simulation results.

Chapter 9

Experimental and Simulation Results

9.1 Introduction

This chapter gives a summary of some of the key results from the experimental work conducted on the two laboratory prototype drives described in the preceding chapter. Since the proposed control scheme was developed and verified using simulation models presented in earlier chapters, conducting experimental tests was paramount not only to enable validation of these models but also to prove on practical machine & converter hardware that the proposed scheme for the electronic commutator and overall drive system is viable when all the practical implementation issues are considered for both even and odd number stator phase topologies. Due to time and cost constraints, the multilevel topology was not experimentally validated. However, since its main difference from the topologies validated here is mainly due to how the machine phase windings are terminated on the electronic commutator power electronics, the developed machine models and overall control scheme are still valid.

The experimental results measurements presented here were taken using a proprietary controller software tool called Pertu with a sampling time of $280\mu s$ and also using a 4 channel LeCroy Oscilloscope LECROYWR6050 with a sampling rate of 200Mega samples per second. All the measurements were then post processed in Matlab. The simulation results presented are based on the models and control strategy detailed in earlier chapters and implemented in Matlab/Simulink and PLECS.

9.2 Machine Electronic Current Commutation

9.2.1 Current Commutation Modes

Both simulation and experimental tests have confirmed that the electronic commutator can be operated in three modes; natural commutation, forced commutation and a hybrid of natural and forced commutation. Unlike conventional brush commuted dc machines where active control of these commutation modes does not exist, electronic machine phase current commutation brings additional operational benefits and flexibility. The commutator operating mode can be readily controlled by controlling the overlap angle (μ) applied between the electronic commutator switching device being turned OFF and the device being turned ON. Simulation and experimental tests have shown that the amount of overlap required can be computed on the fly based on the machine commutating inductance, motor phase voltage, operating frequency and the magnitude of current to be naturally commutated as per analysis presented in chapter 3. Figure 9.1

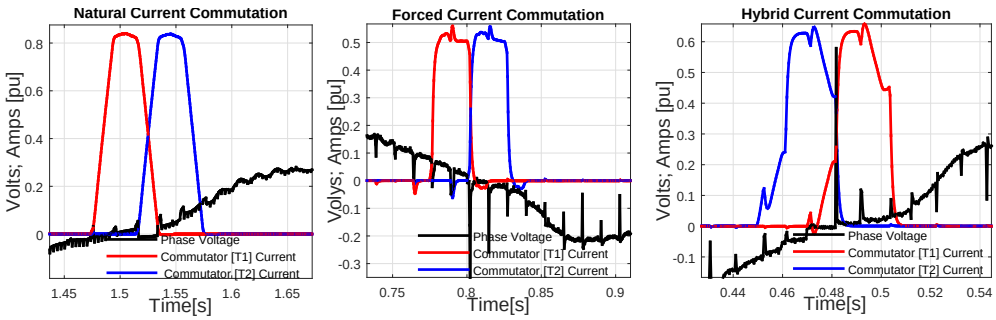

Fig. 9.1 Experimental Measurement: Electronic Commutator Phase Current Commutation Modes; Natural, Forced & Hybrid Commutation

shows experimental measurements taken of the 15 phase prototype drive of the three modes of operation; natural commutation mode where current naturally commutates from T_1 to T_2, forced commutation mode where forced current commutation is used and a hybrid combination of natural and forced commutation where current naturally commutates a given percentage of the current and force commutates the remainder from T_1 to T_2. Figure 9.2 shows simulation results of the three commutation modes. As alluded to earlier, the auxiliary commutation circuits are required to arrest the voltage spikes due to electronic commutator current commutation. Analysis and simulation has shown that the duty and rating of these auxiliary commutation circuits is very dependent

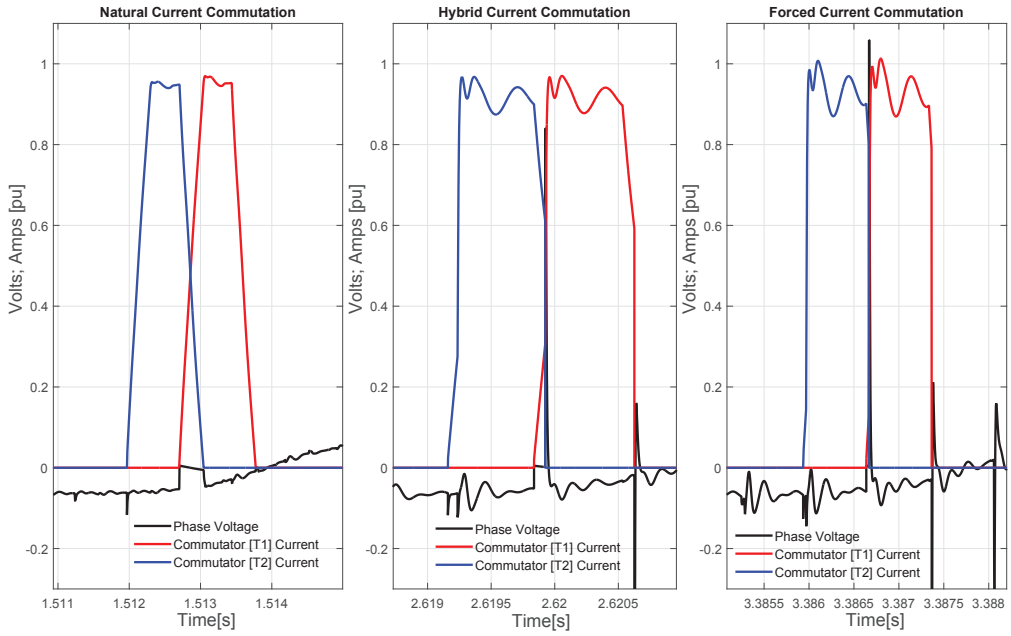

Fig. 9.2 Simulation Results: Electronic Commutator Phase Current Commutation Modes; Natural, Hybrid Commutation & Forced

on the current commutation mode employed. This is clearly illustrated in simulation results depicted in figure 9.3 and figure 9.4 which shows that the current transferred into the auxiliary clamp circuits increases with the level of force commutated current. This is due to the fact that for a given commutating inductance, the energy transferred to auxiliary voltage clamping circuits under forced commutation is proportional to the square of the force commuted current magnitude. It can be seen that with natural commutation, there is hardly any current transfer into the clamp capacitors. As such, the auxiliary switching circuits are essential when forced or hybrid current commutation is employed to arrest the voltage spikes induced as per Lenz's law during forced current commutation where the rate of change of current is very high. Thus, a design compromise is necessary with regard to the size of the auxiliary clamping circuits and maximum current to be force commutated. In this respect, its clear that the natural and hybrid commutation modes can be beneficially exploited to optimise the power electronics design.

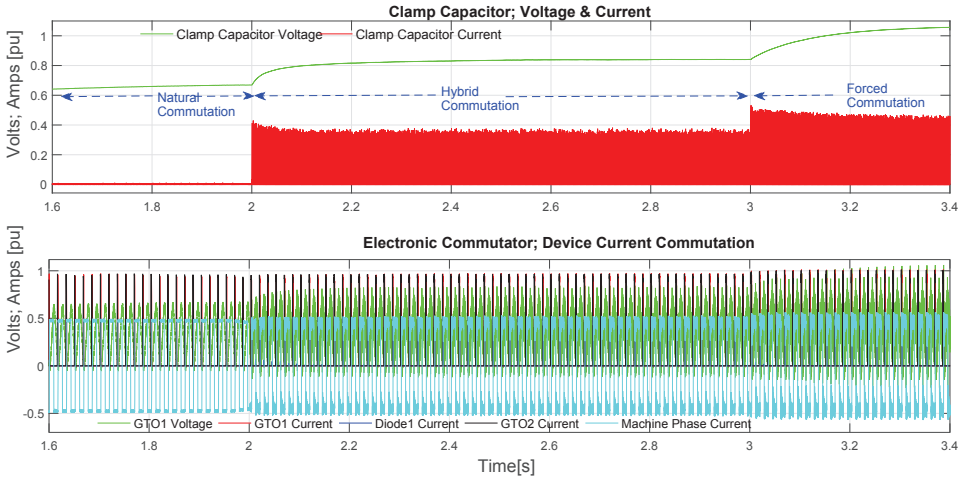

Fig. 9.3 Simulation: Electronic Commutator Commutation Mode Change Effect on Auxiliary Clamp Circuit Current

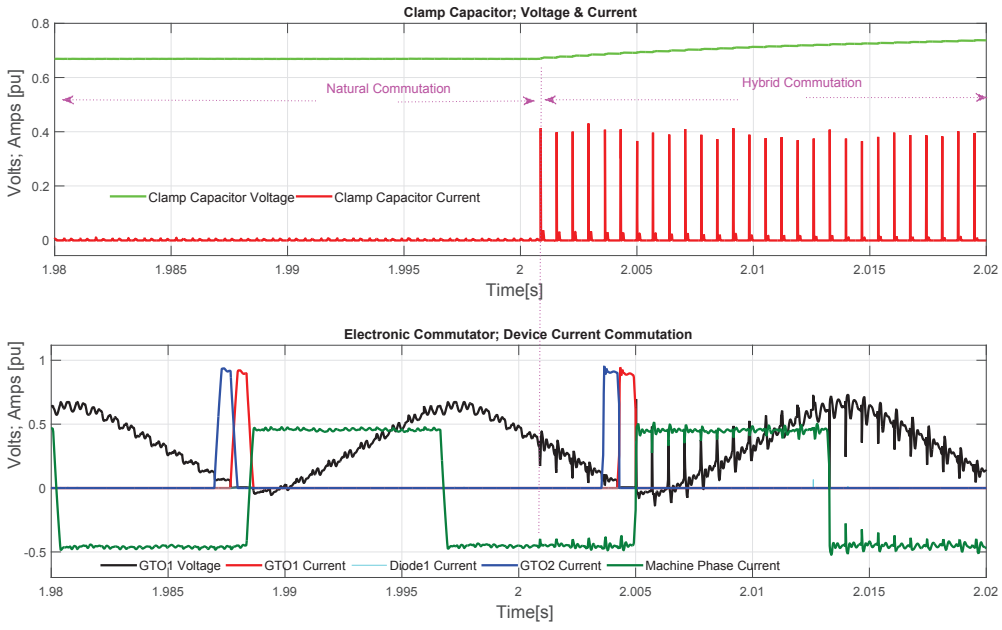

Fig. 9.4 Simulation: Electronic Commutator Commutation Mode Change Effect on Auxiliary Clamp Current

9.2.2 Effect of Electronic Commutator Overlap Angle (μ)

In applications where limitations are imposed on maximum force commutation current, controlling the commutation overlap angle can be used to ensure the switching devices are operated within their designed safe operating area. Figure 9.5 shows experimental measurements on a 15 phase machine taken at fixed 80% speed, 60% flux, with commutator firing angle of 2.62 radians, and at different commutator overlap angles of $\mu = 0.13$ radians & $\mu = 0.03$ radians. It is clear from this figure that the bigger

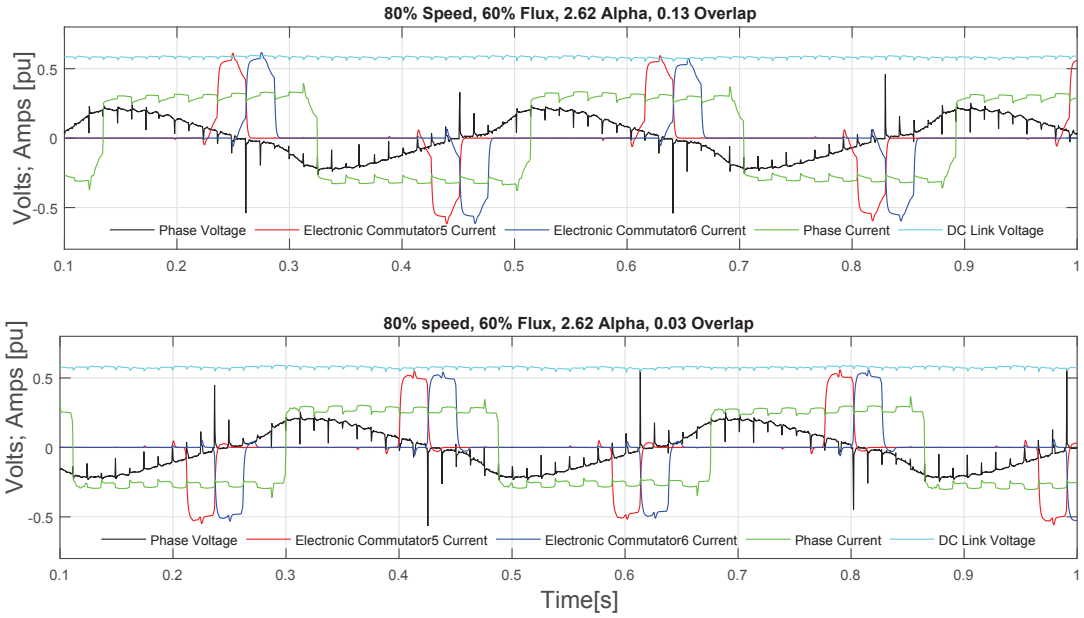

Fig. 9.5 Experimental Measurement: Motoring Mode; Effect Varying Commutation Overlap

the μ, the lower the percentage of the actual phase current that undergoes forced commutation. It is also clear that bigger μ leads to a loss in overall power output as can be seen by the shape of the phase current with triangular edges rather that square edges where the phase current reverses polarity. This loss of power is due to the fact that larger μ extends the commutation interval, hence loss of volt-seconds when the phase undergoing commutation is short circuited and not contributing to machine torque production.

The benefits of using larger μ are in the reduction of the energy transferred to the auxiliary commutation circuits owing to the reduced $0.5L_c i^2$ due to reduced forced commutation current. Additionally, large μ can be exploited in controlling the actual amplitude of switching devices forced commutation current level, particularly in cases where devices with unit gain turn off capability are employed. As such, overlap angle control can be gainfully exploited to minimize auxiliary commutation circuits footprint and also ease switching device duty and gating requirements, albeit at slight loss of machine power output.

9.2.3 Effect of Commutator Firing Angle (α)

The electronic commutator firing angle (α) effectively controls the operating state of not just the electronic commutator but the machine. Not only does it dictate the operating power factor of the machine, it also influences the power losses in the electronic commutator at any given operating point. This is due to the fact that for a given machine operating speed and flux level, varying α causes consequential changes in the amplitude of both the dc link current and voltage for a given operating power level. This effect is depicted in figure 9.6 which shows measured voltages and currents at same operating speed (80%), same machine flux(60%), same $\mu = 0.03$ radians but at different values of α of 2.62 radians and 2.3 radians, for the same per unit output power on a 15 phase machine prototype.

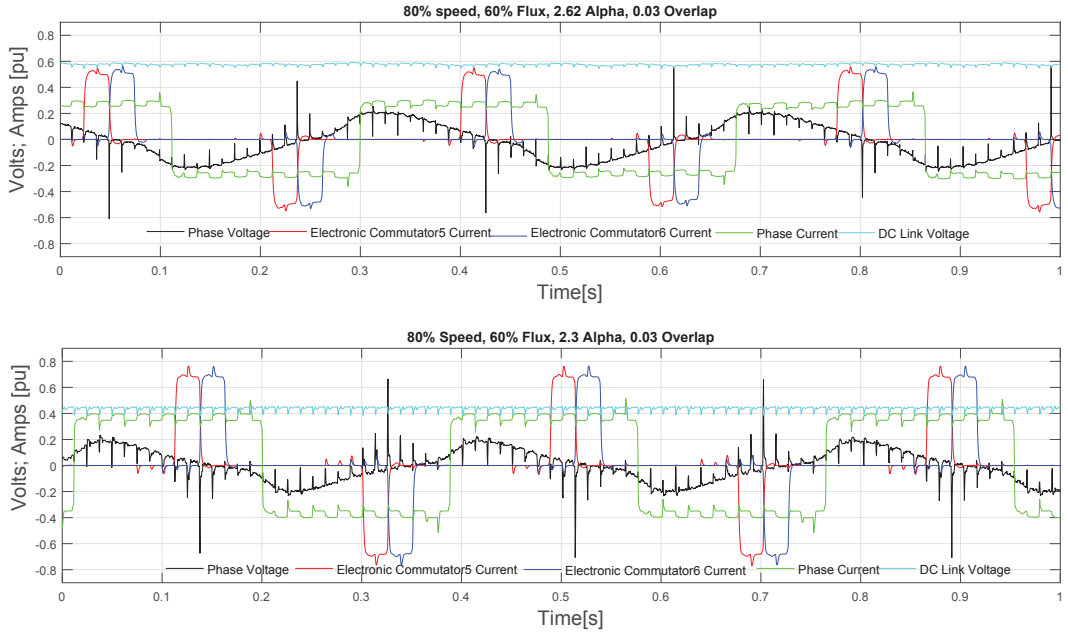

Fig. 9.6 Experimental Measurement: Motoring Mode; Effect Varying Commutator Firing Angle α

The higher the α, the closer the commutator is injecting current near the machine q-axis. A safety margin of 1 to 3 degrees should be allowed to ensure commutation failure does does not occur if devices with no forced commutation capability is used. Firing angles close to the q-axis consequently leads to a higher dc link output voltage and lower machine armature current per given operating power level as depicted in figure 9.6. This potentially improves the efficiency of not just the motor but also the

electronic commutator as ohmic losses are minimised due to the current reduction. Furthermore, owing to the low device switching frequencies inherent in this topology where electronic commutator devices switch at machine fundamental frequencies, switching losses are less dominant compared to conduction losses. Figure 9.7 shows measured electronic commutator device switching and conduction power losses on the 24 phase machine prototype during forced current commutation.

It must be borne in mind that the auxiliary switching circuit losses also increase with increasing current. As discussed in chapter 3, during forced current commutation, the commutating phase current is diverted into the auxiliary clamp circuit diodes which incur switching losses. The losses in the auxiliary commutation diodes are predominantly switching losses and device reverse recovery losses can be dominant. The reverse recovery losses are also dependent or the rate of change of the current being commutated and thus affected by the commutating inductance of the circuit. Figure 9.7 shows measured commutator switching device and auxiliary circuit diode currents during forced current commutation. Its worth highlighting that during current commutation depicted in this figure, some of the current will divert into the incoming device, which is not shown in figure 9.7.

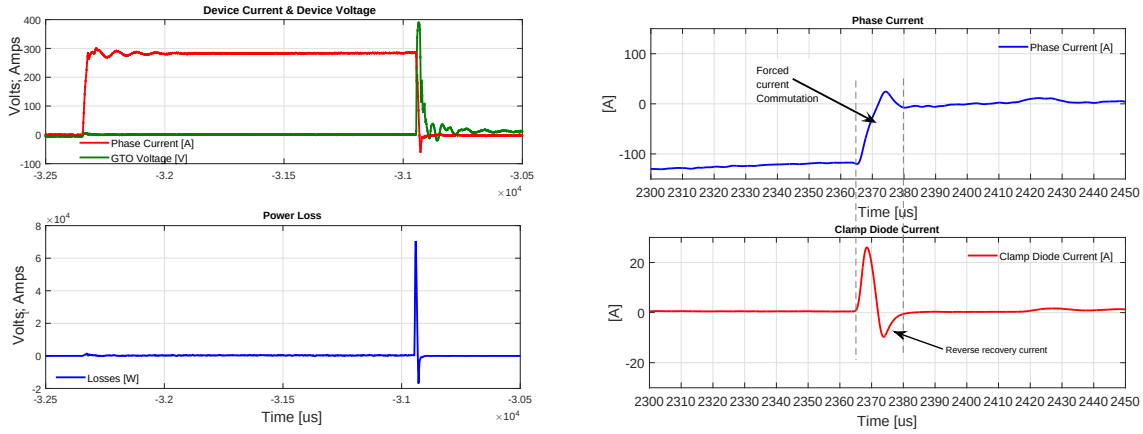

Fig. 9.7 Experimental Measurement: Left; Electronic Commutator Device Commutation Losses, Right; Electronic Commutator Forced Current Commutation Transition Between Switching Device and Auxiliary Clamping Diode

9.2.4 Effects of Armature Reaction

It has been highlighted earlier that armature reaction influences the machine airgap flux and stator back emf voltage waveforms. This also affects the phase voltage available to aid stator phase current commutation as discussed in chapter 3. Figure 9.8 shows the measured waveforms on the 24 phase and 15 phase machine prototypes when operating in generating and motoring modes respectively, highlighting the impact of armature reaction on the stator phase voltages.

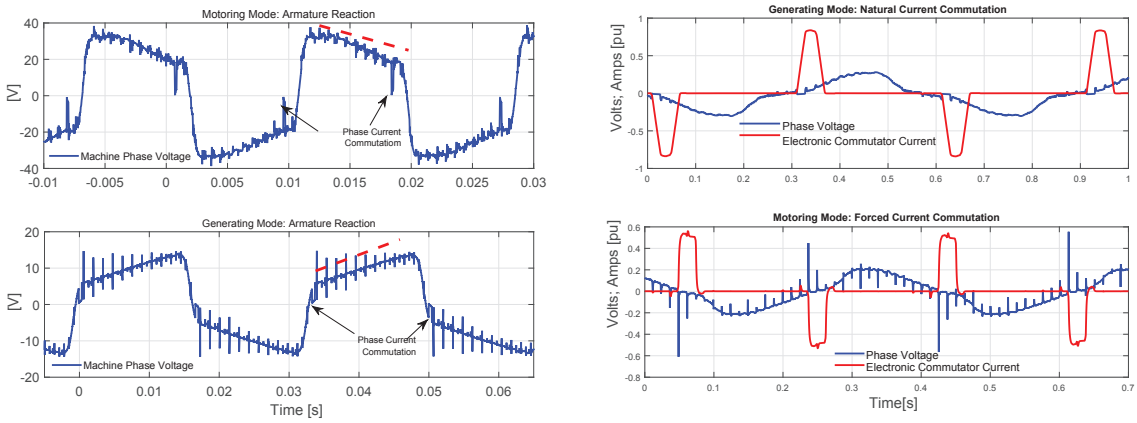

Fig. 9.8 Experimental Measurement: Armature Reaction Effects for Motoring and Generating Modes; Left: 24 phase machine, Right: 15 Phase Machine

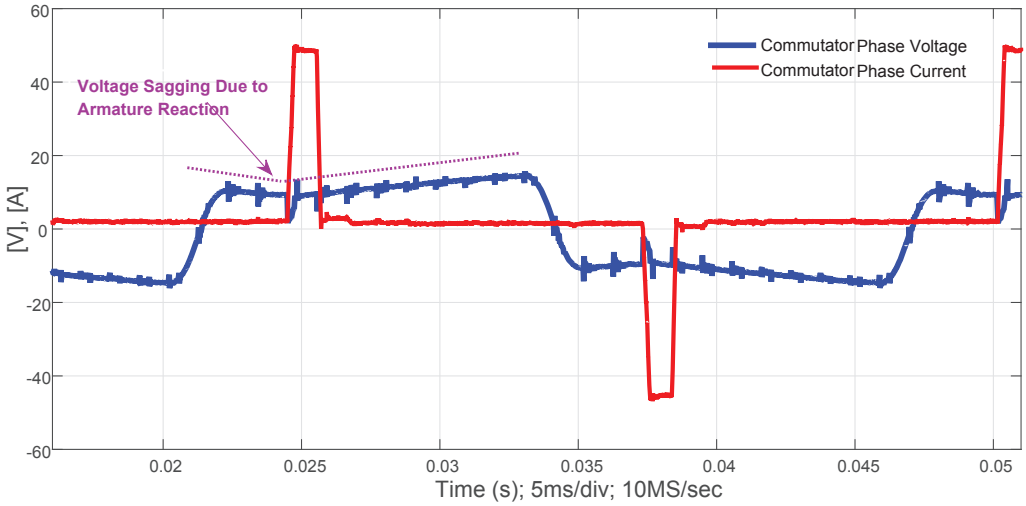

Fig. 9.9 Experimental Measurement: Armature Reaction Effect on Stator Phase Voltage

Armature reaction causes the asymmetry in the phase voltage waveforms where, in the motoring mode the leading edge amplitude is bigger that the trailing edge and vice versa for the generating mode. This results from the fact that the injected stator current creates a flux distribution that acts to weaken and distort the main airgap flux setup by the rotor field at the position where the current is injected relative to the rotor flux position. This means the net resultant flux and induced stator back emf is weaker at the vector position where stator current is injected. This results in a linear reduction of stator terminal voltage amplitude as depicted in figure 9.8. Its clear that the worst flux distortion corresponds to the relative position where the stator phase current is injected. This means when the stator current is injected further away from the q-axis, sagging of the stator voltage results as clearly depicted in the measured phase voltage in figure 9.9 which shows commutator phase current and machine phase voltage at $\alpha = 0.70$ radians. Armature reaction can be minimised by machine design if the reluctance of the path of the cross-magnetising field is increased. The armature teeth and air gap at pole tips offer reluctance to armature flux. Thus by increasing length of air gap, the armature reaction effect is reduced.

9.2.5 Measurement of Commutating Inductance

The impact of machine commutating inductance on electronic commutator phase current commutation was analysed and highlighted in earlier chapters. One of the experimental validation aims was to explore the impact of rotor damper windings on the machine commutating inductance with a view to find ways of minimizing the machine commutating inductance. Measurements taken on a 24 phase prototype machine with and without a rotor damper winding in the form of a cylindrical rotor copper can confirmed that rotor damper windings can yield a significant reduction in commutating inductance. The inductance is calculated as per Lenz's law from the measured commutation voltage and rate of change of current during commutation as discussed in earlier chapters. Figure 9.10 shows the measured commutating inductance of 124μH without the rotor cylindrical damper. Figure 9.11 shows the measured machine commutating inductance of 29μH with a cylindrical rotor copper can damper

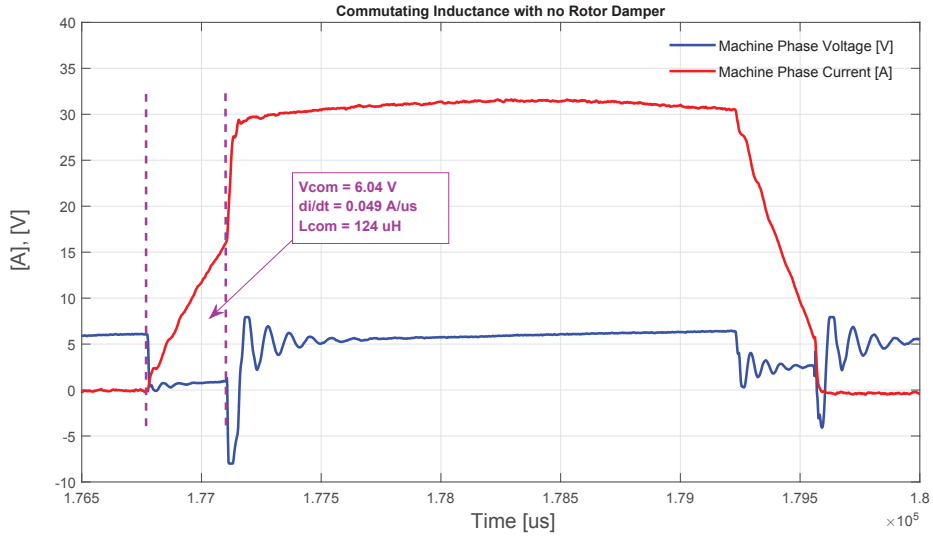

Fig. 9.10 Experimental Measurement: 24 Phase Machine Commutating Inductance with no Rotor Damper Can

winding. It is clear that the rotor damper winding resulted in a 76% reduction in the machine commutating inductance.

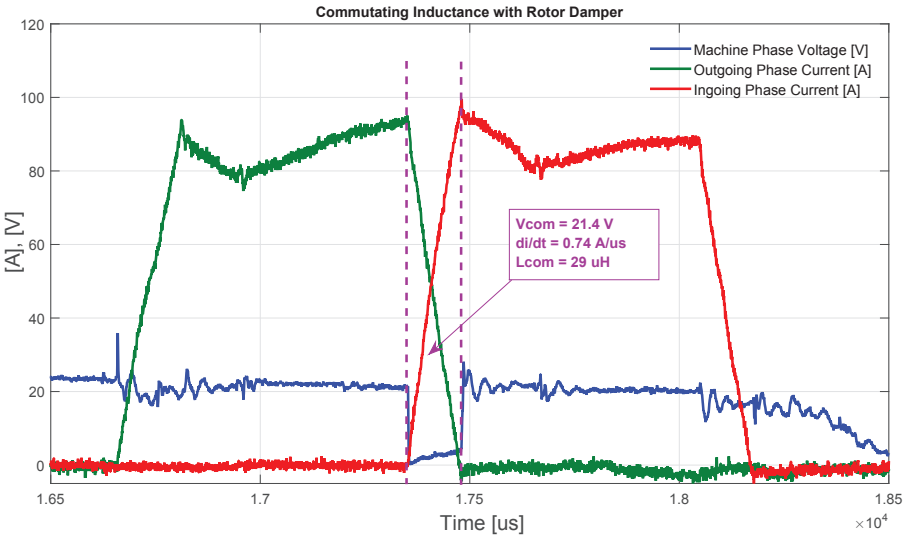

Fig. 9.11 Experimental Measurement: 24 Phase Machine Commutating Inductance with Rotor Damper Can

Figure 9.12 shows the simulation results which show close agreement to the practical measurement results for the machine with rotor damper winding and also confirms the suitability of the method used to measure the commutating inductance.

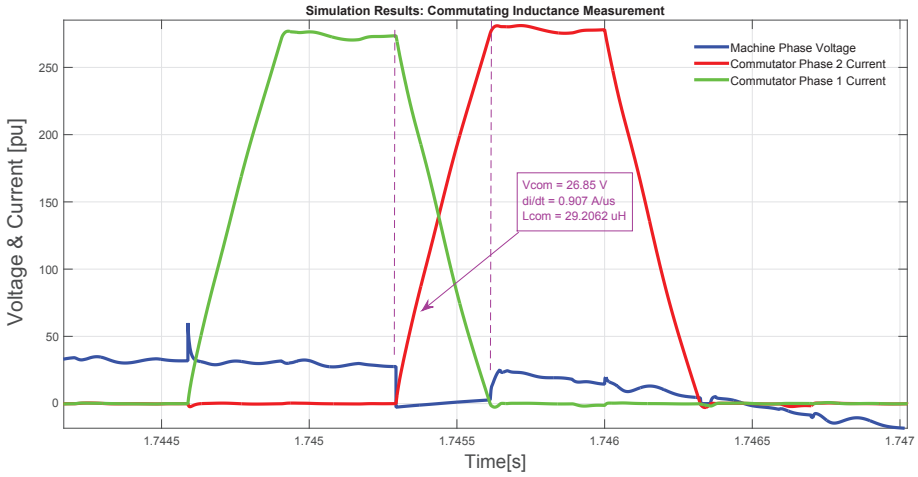

Fig. 9.12 Simulation: Commutation Inductance Measurement

9.2.6 Commutation Circuit Loop Inductance

It was generally known through analysis and simulation that the electronic current commutation process is inductively dominated. This means, it is not only affected by the commutation inductance but also by the effective loop inductance of the circuit undergoing commutation.

One of the key protection strategies proposed for detecting electronic commutator faults is through parity monitoring of the auxiliary clamp capacitor voltages. This strategy works well on the assumption that the machine and loop impedances are balanced between machine phases. Experimental results have confirmed that the loop inductance due to cabling between the electronic commutator power electronics and the machine can adversely affect current commutation and consequently the viability of the proposed protection strategy if the loop impedances are grossly unbalanced.

Figure 9.13 shows the measured clamp capacitor voltages on the 24 phase machine prototype. The effect of unbalanced loop inductances can be clearly seen as highlighted divergence of the two auxiliary circuit clamp capacitor voltages. Each voltage peak corresponds to a phase current commutation, as such it can be seen that phase 3,4,7,9,10,& 11 have unbalanced loop inductances, where phase one is assumed to be at the start of the fundamental machine rotor position angle in figure 9.13. However, in this case the loop inductance imbalance was not significant. Simulation results where loop inductance imbalances were deliberately introduced clearly shows this effect not just on clamp capacitor voltages but also on the commutating current $\frac{di}{dt}$ as depicted in

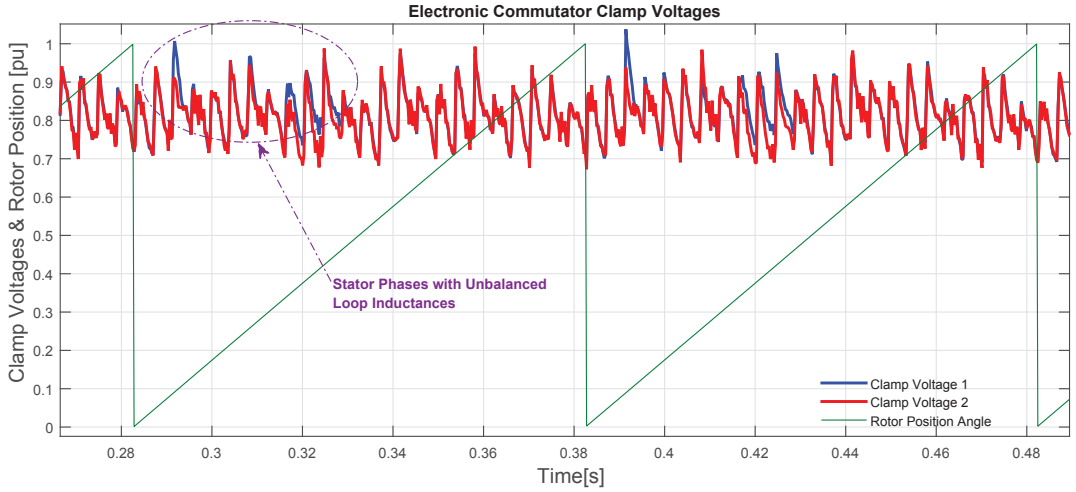

Fig. 9.13 Experimental Measurement: Effect of Unbalanced Loop Inductances on Clamp Capacitor Voltages

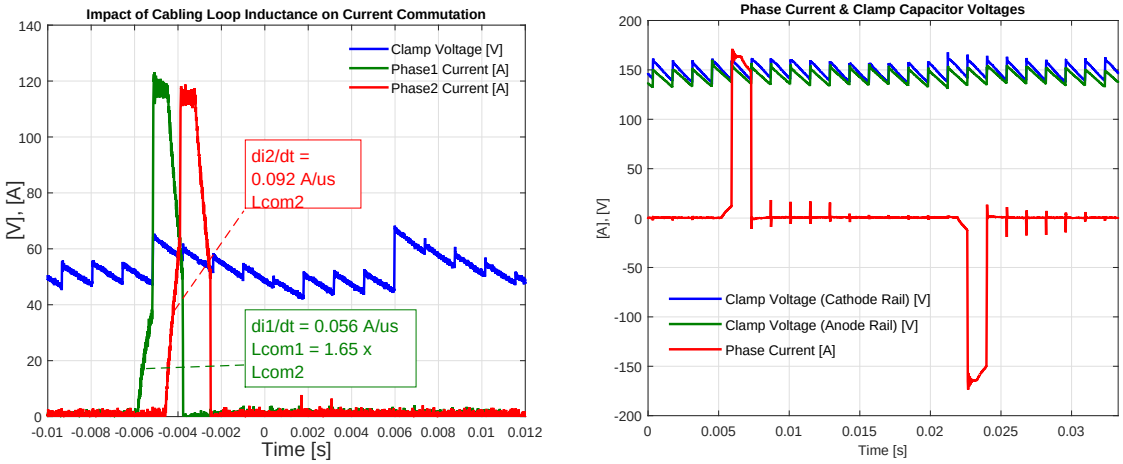

Fig. 9.14 Simulation Results; Left: Impact of Cabling Loop Inductance on Current Commutation, Right: Impact of Cabling Loop Inductance on Clamp Capacitor Voltages

figure 9.14. The differences in the effective loop inductances of the respective phases results in different rates of change of current during commutation events and also the amount of energy transferred to the auxiliary clamp capacitors. One conclusion drawn from this is that careful attention should be given at design stages to ensure balanced loop impedances between electronic commutator and machine phases.

9.2.7 Clamp Capacitor Voltage Parity Protection

Analysis of the electronic commutator circuit operation and simulations have shown that all electronic commutator and machine faults result in changes that can be detected via measurement of the auxiliary clamp circuit voltage imbalances. Indeed one such electronic commutator fault was experienced on the 24 phase prototype drive during experimental tests when an electronic commutator switching device snubber resistor failed. The failure created a short circuit across an electronic commutator phase switching device resulting in undesirable current path causing the clamp capacitor to rapidly charge up compared to the other clamp capacitor. The divergence in measured clamp capacitor voltages can be clearly seen in the measured clamp capacitor voltages in figure 9.15. The clamp capacitor parity voltage protection was effective at detecting and shutting down the electronic commutator.

9.3 Proposed Control Scheme Measured Performance Results

The key aims of the experimental test rigs alluded to in the preceding chapter include; (a) validation of the proposed control strategies for electronic current commutation of the multiphase machine topologies, particularly the electronic commutator power electronic topology and how it is actively controlled to mimic the behaviour of mechanical commutation process of conventional dc machines; (b) validating the overall drive control strategies to ensure full four quadrant operation and (c) to fully characterise the transient, dynamic and steady state performance of the overall drive system, i.e. machine, power electronic converter and control system, over the entire drive torque/speed operating range. The measurement and simulation results presented in

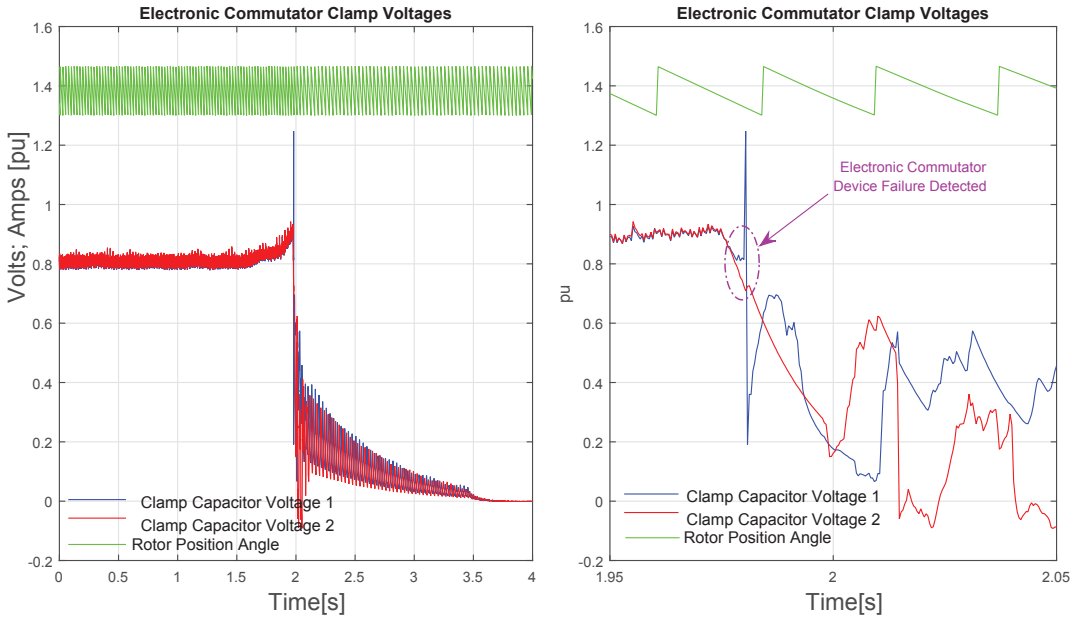

Fig. 9.15 Experimental Measurement: Left:Electronic Commutator Device Snubber Circuit Failure Detection by Clamp Capacitor Parity, Right: Zoomed of Figure

the following sections demonstrate that the proposed scheme meet all the key aims outlined above.

9.3.1 Transient Performance

A key challenge was to develop a scheme that ensures electronic commutator control of the machine whilst maintaining synchronisation with the rotor flux position through fast transient changes such as fast speed reversals, fast speed ramp rates and rapid machine torque reversals. Simulation and experimental tests have confirmed that the proposed control scheme yields good transient response as highlighted in earlier discussions in chapter 7.

Fast Speed Reversals & Step Changes

Obviously the design of outer control loops like speed controllers holds on the assumption that the inner control loops such as dc link current control and electronic commutator control deliver the demanded performance. As such, good speed control performance can only be guaranteed if all the inner control loops behave as expected. Figure 9.16 shows the measured machine speed reversal for positive to negative speed

reversal and vice versa. The rate of change of speed is mainly dominated by the mechanical drive train inertia and maximum torque rating of the machine and its converter. The results show that the electronic commutator successfully controls its firing angle to deliver the required torque whilst at the same time remaining synchronised to the machine flux vector position. Figure 9.17 shows the measured machine speed controller response to step changes in the reference signal. In this test, the speed controller peak output torque demand was limited to 40% and machine was coupled to a load machine , and had to overcome the drive train inertia. The results show that the outer speed control loop and the inner dc link current and electronic commutator control loops give good transient performance.

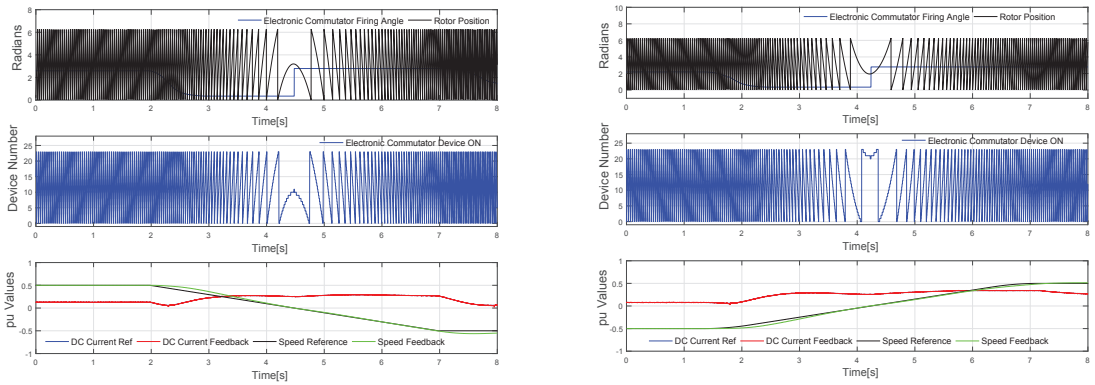

Fig. 9.16 Experimental Measurement: 24 phase Machine Speed Reversal. Left; Positive to Negative Speed, Right; Negative to Positive Speed

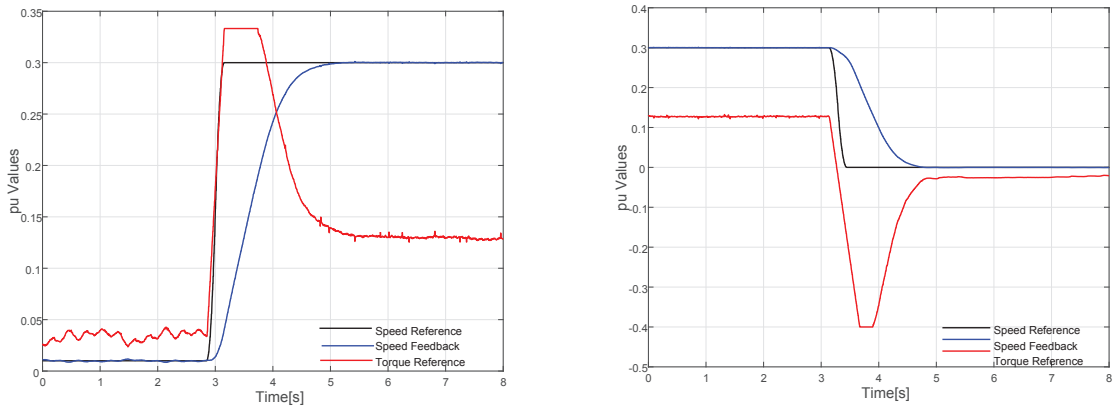

Fig. 9.17 Experimental Measurement: 24 phase Machine Speed Reference Step changes. Left; Positive Speed Step Change, Right; Negative Speed Step Change

Fast Torque Reversal Changes at Fixed Speed

To evaluate the performance of the proposed control scheme to fast transient machine torque reversal changes, the 24 phase machine prototype regenerative drive was configured with the load machine operating at fixed speed and the drive under test was subjected to very fast torque transients. In this test the speed controller of the drive under test was bypassed and a fast torque reference command was send to the dc link controller and electronic commutator controller. It should be noted that only speed control scheme has been discussed in the control scheme presented. In this case the speed controller outputs a torque reference from which the torque producing current component is computed by dividing the torque reference by the machine flux magnitude. For this test an open loop torque reference ramp command was used in the experimental shown. Figure 9.18 shows the measured machine fast torque reversal from -1.0 pu negative torque to 1.0 pu positive torque reversal in 1.0 seconds and vice versa. The experimental results clearly shows that both the dc link current controller and electronic commutator control delivers robust performance. A machine dc link voltage feed-forward term was included in the dc link current controller output to enable fast dc link current reference tracking in the presence of rapid dc link voltage changes caused by the rapid electronic commutator quadrant change phase control.

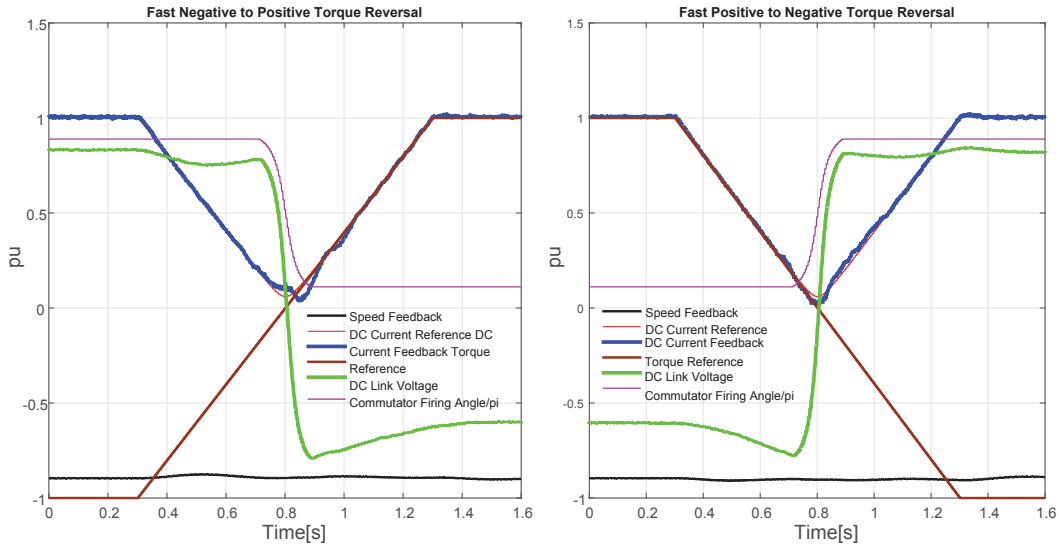

Fig. 9.18 Experimental Measurement: Machine Torque Reversal at Fixed Speed

Figure 9.19 shows the variation of dc link voltage and current with machine torque during torque reversal. Unlike brush commutated dc machines where quadrant changes are effected by dc link current reversal which requires two anti-parallel bridges, here quadrant changes are accomplished by electronic commutator phase control which acts to reverse the dc link voltage. These measured waveforms clearly show that the electronic commutator control can cope with very fast torque reversals, proving the robustness of the implemented scheme. Its worth noting that when this drive topology is connected to a common dc power system, a dc/dc converter is required to; (a) decouple the machine dc link from the common dc to enable machine output dc voltage reversal during quadrant changes and (b), to control the machine dc link current amplitude. As discussed in the *MT*-axis reference frame control scheme formulation, it can be seen from figure 9.19 that the machine torque is directly proportional to the DC link current. Thus, the dc link current controller and electronic commutator controller can selectively influence machine torque independently from machine flux controller.

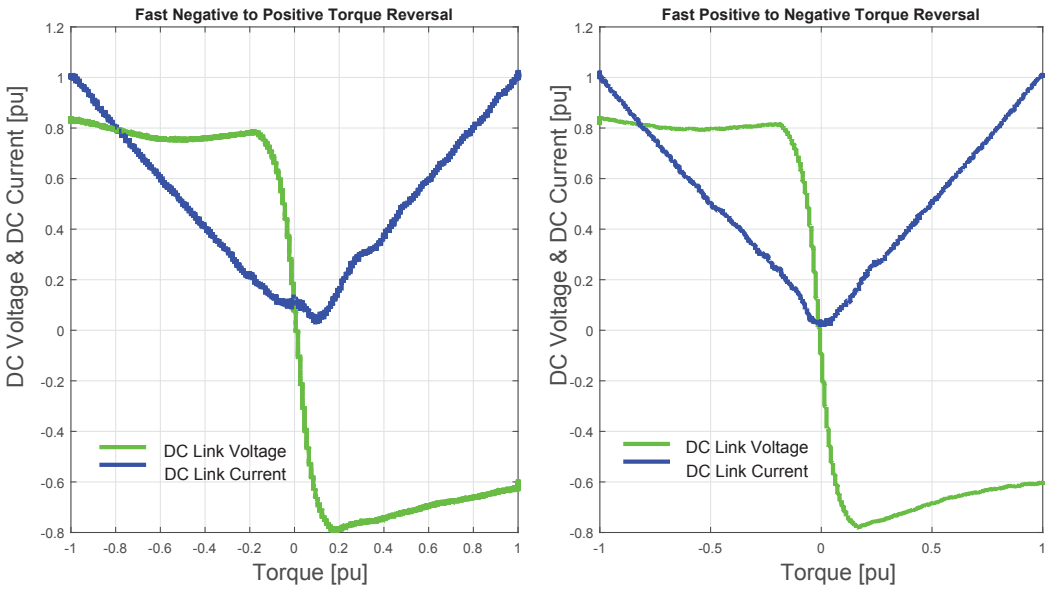

Fig. 9.19 Experimental Measurement: Torque Reversal; Variation of DC Link Voltage and Current with Machine Torque

9.3.2 Steady State Performance

Tests were carried out at various speeds and power levels to validate the steady state performance characteristics of the drive, and verify stable operation of the drive control

loops and electronic commutation control. The experimental results confirmed the results obtained via simulation that stable operation is achieved over the entire machine torque speed profile.

Steady State Operation with Forced Current Commutation

Figure 9.20 shows the measured waveforms taken on the 24 phase prototype during steady state operation at rated speed and maximum power. The field current was limited to 95% due to rotor field thermal limit of the experimental drive. The top plot shows the dc link voltage and the electronic commutator phase current operating in hybrid commutation mode. Hybrid commutation mode was used at high current because the electronic commutator devices employed could only commutate 90% of the rated current. The bottom plot shows the dc link voltage and the corresponding machine phase voltage waveforms. The forced current commutation voltage spikes are evident on the machine phase voltage waveform. The commutation notches on

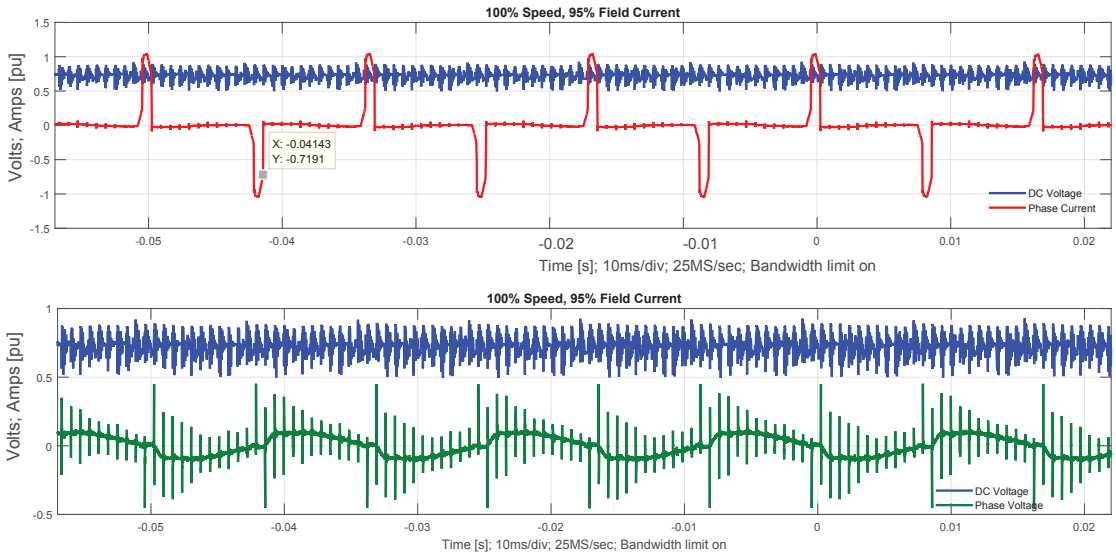

Fig. 9.20 Experimental Measurement: Steady State operation with Forced Commutation

the dc link voltage were mainly due to the selective harmonic elimination PWM scheme used on the network converter. Figure 9.21 shows the dc link voltage measured on the network converter and machine side of the dc link reactor. As per analysis presented in earlier chapters on the benefits of diminished low order harmonic of multiphase machines inspite of the electronic commutator operating at very low

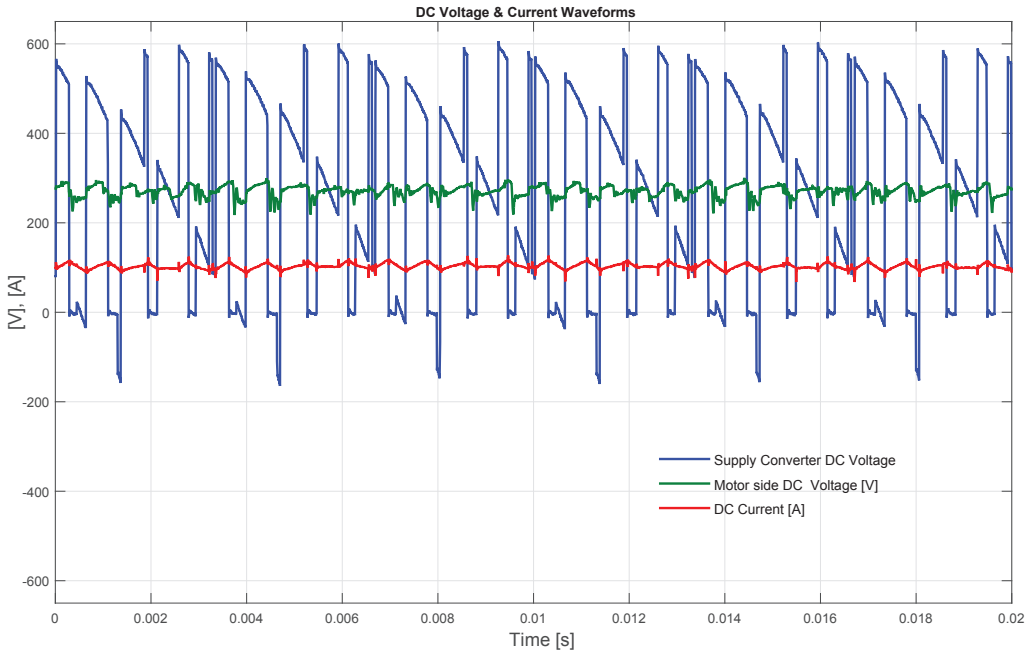

Fig. 9.21 Experimental Measurement: DC Voltage & Current Waveforms

machine fundamental frequencies, the dominant low order harmonics on the dc link is at 24th & 48th harmonic orders of the machine fundamental frequency for the 24 phase machine prototype. This can be seen in the dc link current measurement and fast fourier transform given in figure 9.22. The 30th harmonic order in this figure is due to the network converter PWM frequency.

Experimental results confirmed stable operation with forced commutation. Forced commutation is analogous to under-commutation in classical dc machines where the brush gear disconnects from Commutator segments before the current goes to zero, which results in brush gear sparking as discussed in chapter 2. Clearly, electronic commutator control facilitates stable operation in under-commutated mode and circumvents the undesirable drawbacks of classical dc machines for the same operating mode. This demonstrates that the electronic commutator power devices can tolerate under-commutation without sparking as the gate turn on/off process displaces the sparking that would otherwise occur in mechanical commutators.

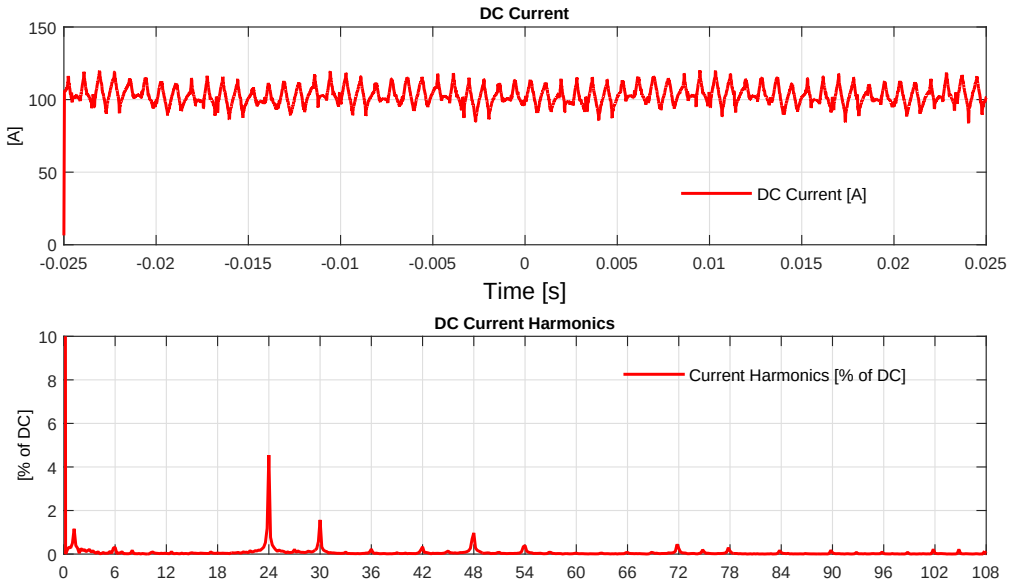

Fig. 9.22 Experimental Measurement: DC Link Current Harmonics

Steady State Operation with Natural Current Commutation

Operation in natural commutation also confirmed that the electronic commutator can tolerate over-commutation without sparking because the commutator power semiconductor switching device reverse recovery blocks the current reversal that would otherwise be interrupted by brush commutator action. Figure 9.23 shows measured waveforms for natural operation. The top plot shows the voltage across the electronic commutator switching device and the corresponding commutator phase current. The bottom plot shows the measured dc link voltage and machine phase voltage waveforms. In comparison to the force commutation measurements given in figure 9.20, the absence of significant commutation spikes on the phase voltage can be clearly seen with natural current commutation. Figure 9.24 and figure 9.25 shows similar results from simulation results of natural and forced commutation operation of the 24 phase machine topology showing stable steady state operation. In steady state and when no commutation events are occurring, the machine phase mutual coupling between machine phase windings has no effect on adjacent windings. This is due to the fact that the machine current is dc when the phase is not undergoing commutation, as such, inductive mutual coupling effects are completely decoupled between adjacent phases. However, mutual coupling effects still affects adjacent phases during fast

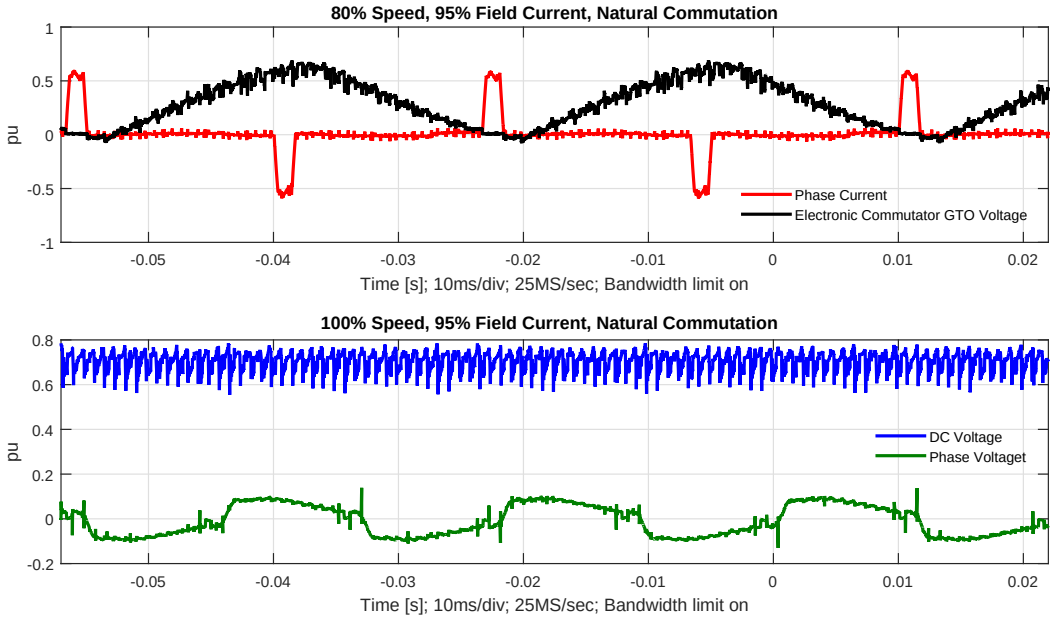

Fig. 9.23 Experimental Measurement: Steady State operation with Natural Commutation

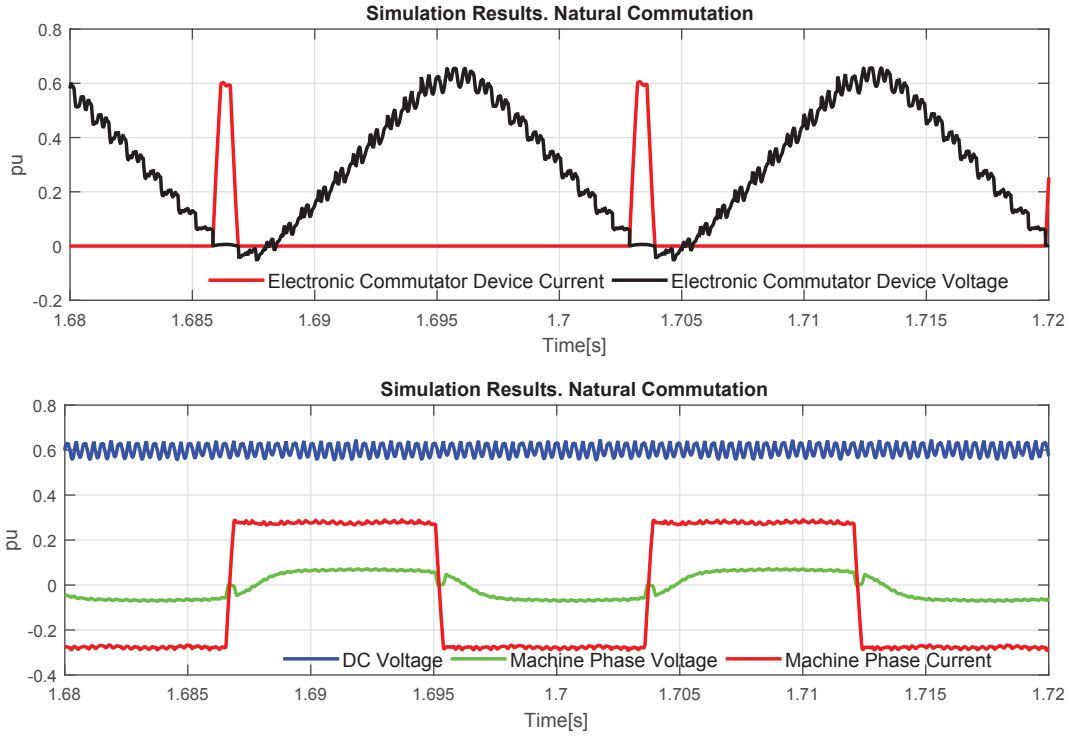

Fig. 9.24 Simulation Results: Steady State Electronic Commutator Natural Commutation Operation

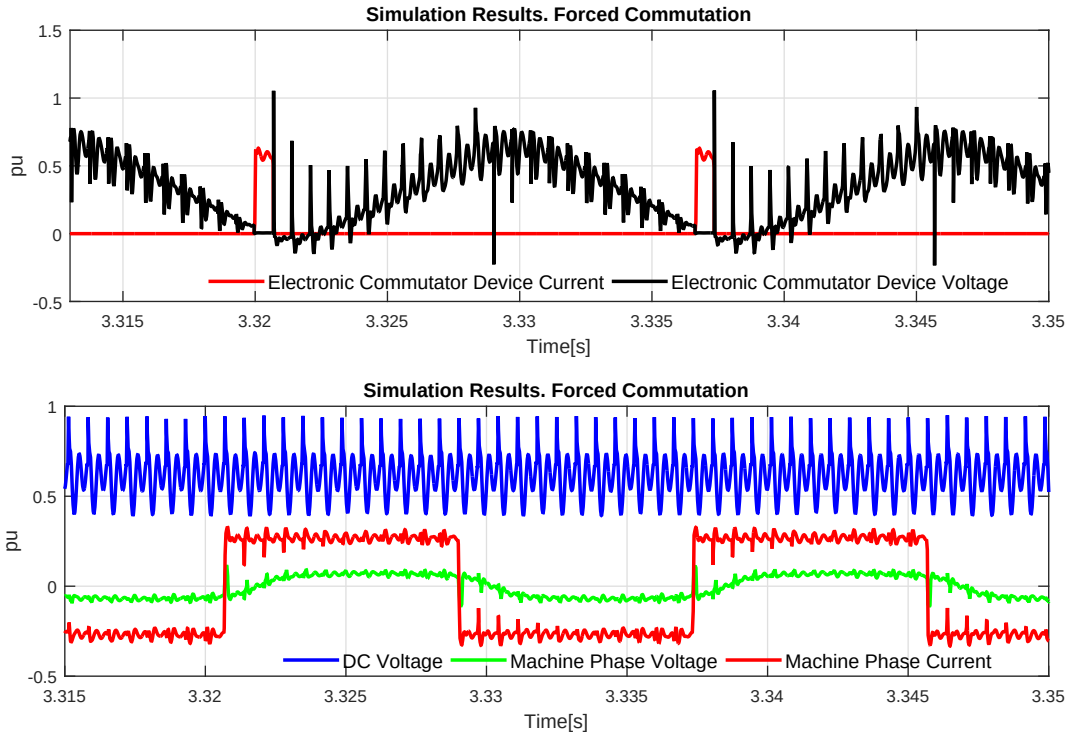

Fig. 9.25 Simulation Results: Steady State Electronic Commutator Forced Commutation Operation

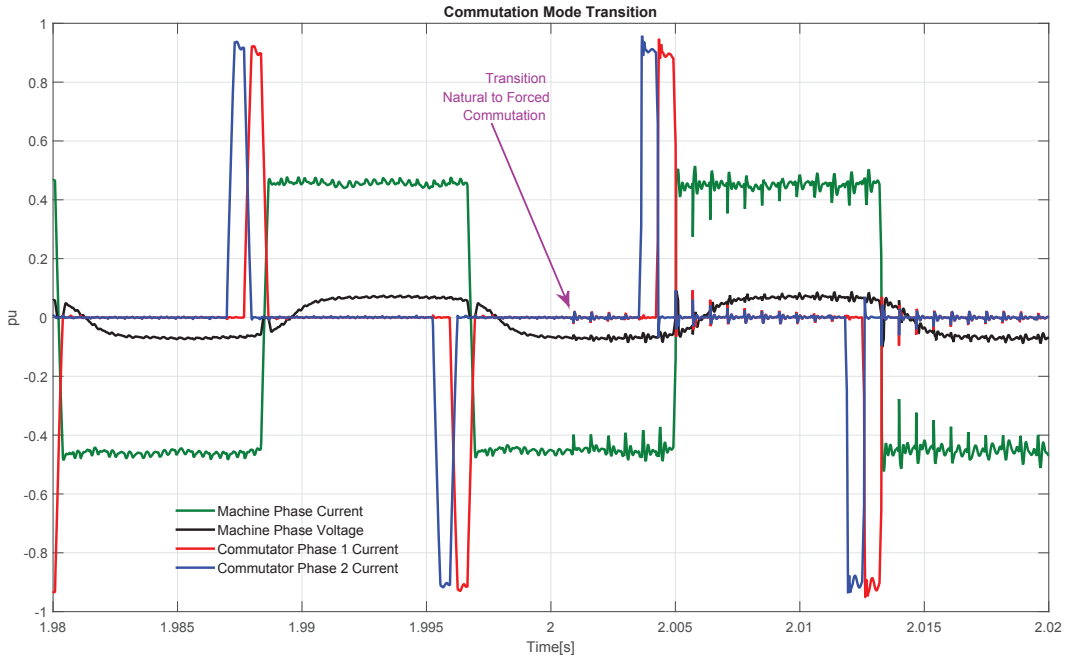

Fig. 9.26 Simulation Results: Mutual Coupling Effects Due to Electronic Commutator Commutation Mode

current commutation events experienced during forced current commutation as can be seen by small current spikes on the phase currents during commutation events on adjacent phases. The induced voltages in the stator phase windings due to mutual coupling act to cause transient forward biasing of the auxiliary circuit clamping diodes resulting in the short current spikes on phase current at commutation intervals. This is illustrated by simulation results of figure 9.26 which shows the increased mutual coupling effect on machine phase current when the commutation mode is switched from natural to forced current commutation. As can be seen, the coupling is strongest due to commutations of adjacent phases and the effect diminishes for phases that are further away. Obviously the rate at which phase current is commutated plays a part and should be considered at the design stage to minimise the impact of these induced harmonics on machine performance. Stable steady state operation was also observed

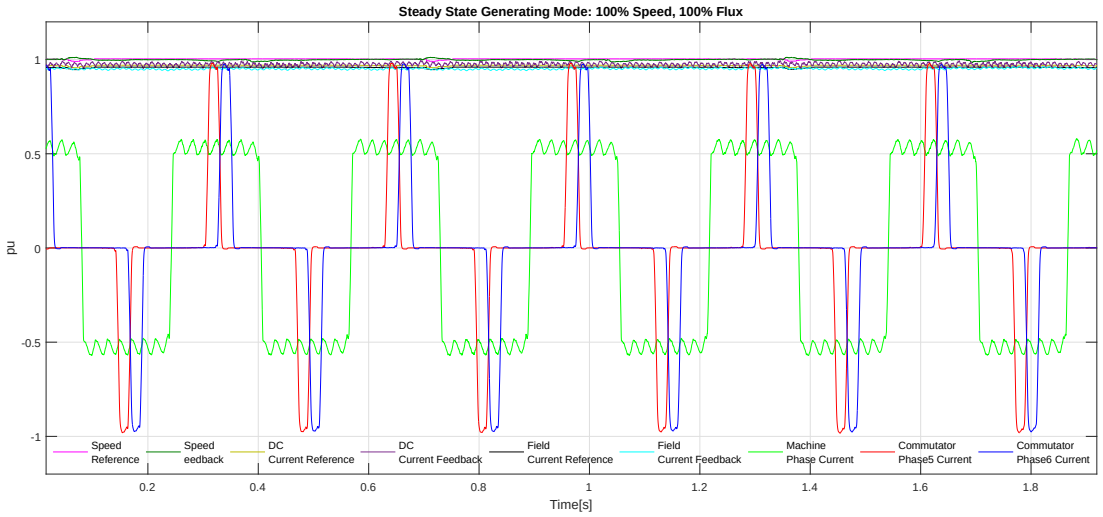

Fig. 9.27 Experimental Measurement: 15 Phase Prototype Machine, Full Load Steady State Generating Mode

on the 15 phase topology as evidenced by the experimental waveforms presented earlier. Figure 9.27 shows experimental waveforms of full speed full power stable operation of the 15 phase machine prototype in generating mode with natural current commutation. All the control loops for speed, flux, field current, dc link current and electronic commutator show stable operation. Figure 9.28, figure 9.29 & figure 9.30 all show stable operation at different speeds, commutator firing angles and generating

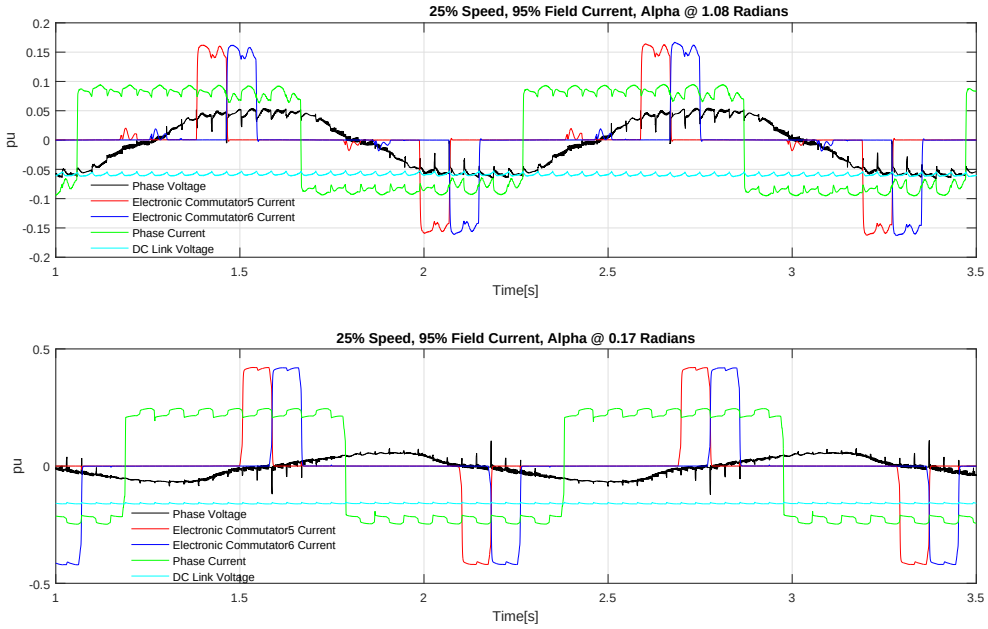

Fig. 9.28 Experimental Measurement: 50% Speed Generating Mode; Varying Electronic Commutator Firing Angle Alpha

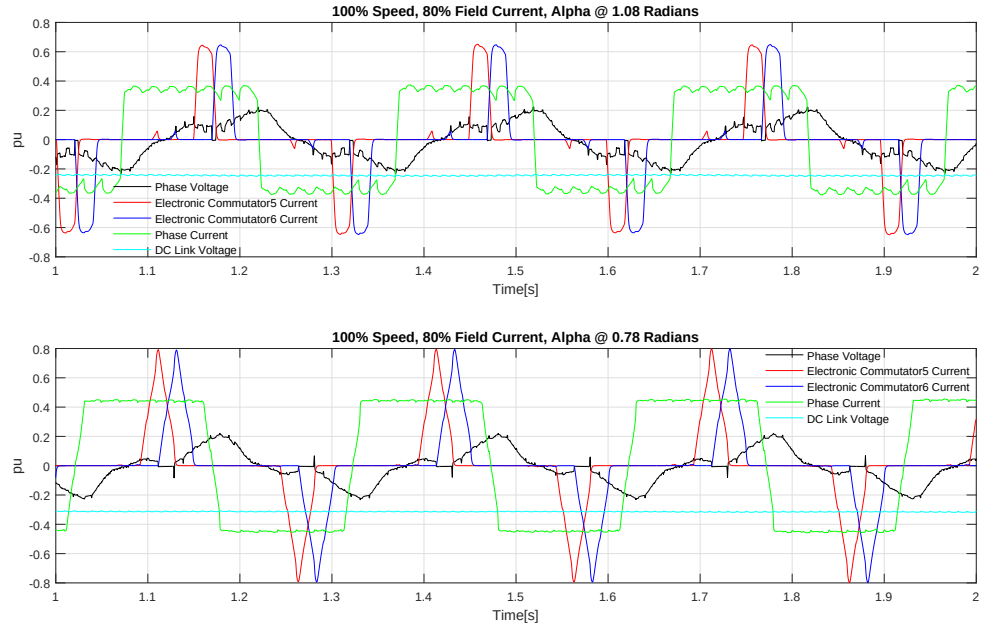

Fig. 9.29 Experimental Measurement: Full Speed Generating Mode; Varying Electronic Commutator Firing Angle Alpha

and motoring modes for the 15 phase machine topology.

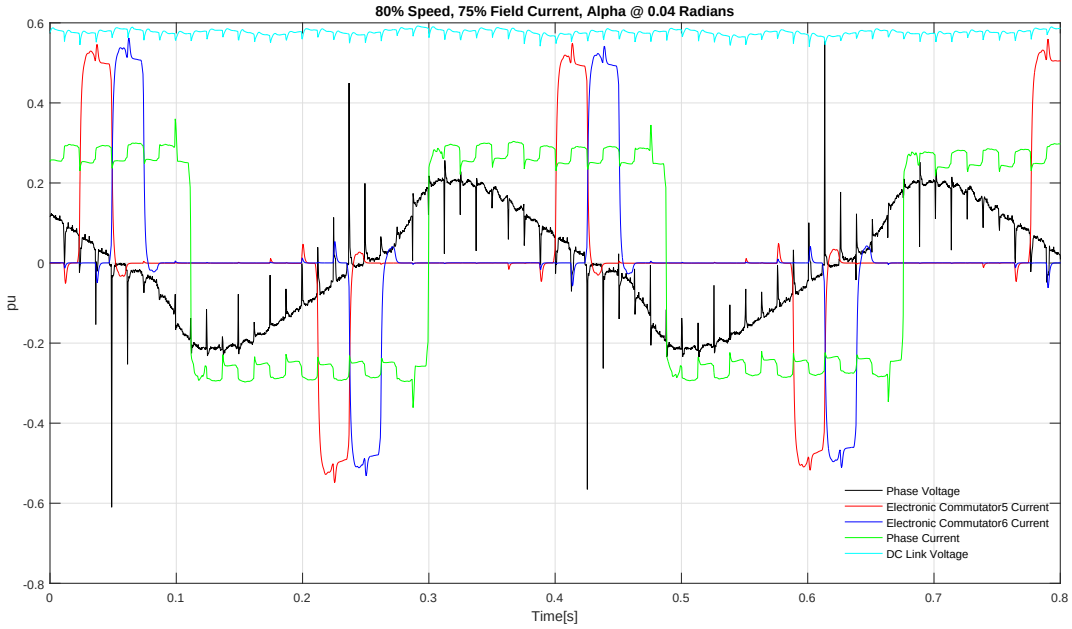

Fig. 9.30 Experimental Measurement: 80% Speed Motoring Mode; Current Commutation at q-axis

9.3.3 Dynamic Performance

Application Case Study: Marine Propulsion Crash Stop

In order to demonstrate suitability of the multiphase electronically commutated dc machine for marine propulsion, a typical ship propulsion load profile is essential [230–232]. Figure 9.31 shows a block diagram representation of the model used to simulate typical marine propulsion torque/speed characteristics. In this model per unit values are used, the speed controller regulates the propulsion motor shaft speed and generates a shaft torque reference from which the propeller speed is calculated using the motor & propeller inertia and propeller torque feedback. The Robinson torque/speed curves compute the propeller torque for different ship speeds. This model was programmed on the load drive of the 24 phase prototype to mimic a typical ship's load profile and used to validate the multiphase electronically commutated dc machine crash stop manoeuvres response. A marine propulsion drive crash stop manoeuvre was chosen owing to its arduous duty which requires very good transient, dynamic & steady state drive control performance. A crash stop manoeuvre is performed to quickly stop a moving ship by reversing the rotational speed of the propeller. This

required the machine and converter to rapidly transition from motoring quadrant to generating quadrant and back to motoring quadrant in the opposite shaft rotations direction. The per unit Robinson equations applied to the model shown in figure 9.31

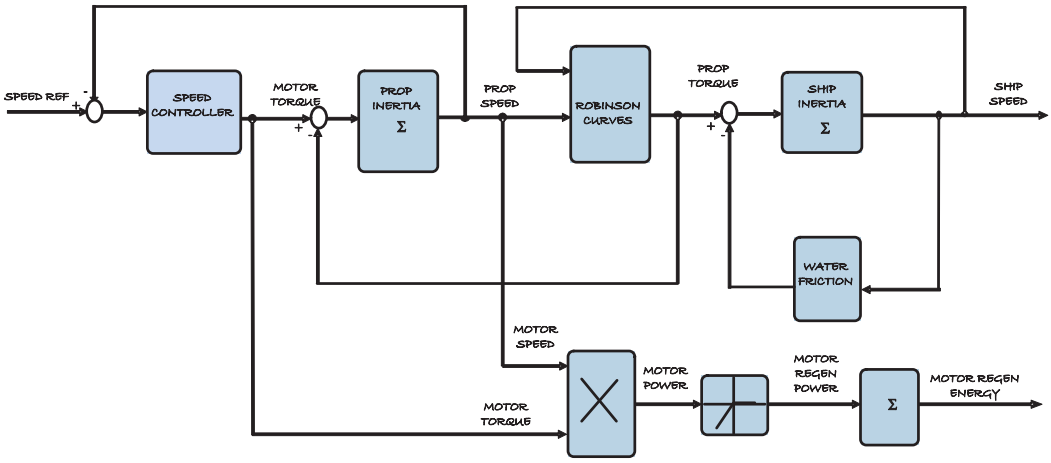

Fig. 9.31 Marine Crash Stop Model Implemented for Dynamic Validation Testing

above are given as;

$$T_{Robinson} = \begin{cases} k_{prop} \times \omega_{prop} \times |\omega_{prop}| - k_{ship} \times \omega_{ship} \times |\omega_{ship}| & \text{if } \omega_{prop} \geq 0 \\ (\omega_{prop} - k_e \times \omega_{ship}) \times \omega_{prop} \times k_d - k_{ship} \times \omega_{ship} \times |\omega_{ship}| & \text{Otherwise} \end{cases}$$

The water friction is modelled by the following equation;

$$T_{Waterfriction} = \begin{cases} \omega_{ship} \times |\omega_{ship}| \times k_{wf} & \text{if } \omega_{ship} \geq 0 \\ -2 \times \omega_{ship} \times |\omega_{ship}| \times k_{wf} & \text{Otherwise} \end{cases}$$

where ω_{ship} is the per unit ship speed, ω_{prop} is the per unit propeller angular speed and the model coefficients used are; $k_{ship} = 1.05$, $k_{prop} = 2.0$, $k_d = 2.5$, $k_{wf} = 0.01$ and $k_e = 0.2$. The load inertia is modelled as a low pass filter whose time constant represents the inertia of the ship in seconds. Figure 9.32 below shows typical propeller torque vs speed curves through time during a crash stop for different ship speeds.

Experimental Results

Figure 9.33 shows measurement of the drive speed, torque and dc link voltage from a real marine vessel driven by an induction motor with a non-regenerative voltage source converter for a crash stop manoeuvre. For a PWM voltage source converter,

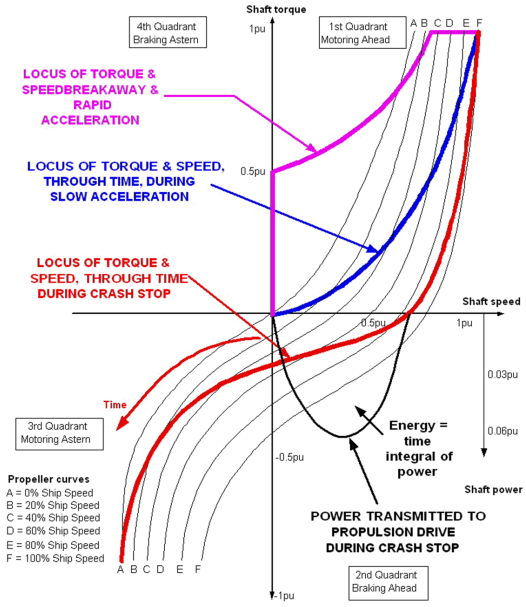

Fig. 9.32 Marine Crash Stop Propeller Torque Speed Curves [Public Domain]

quadrant changes are effected by slip frequency control with unipolar dc link voltage and bi-directional dc link current.

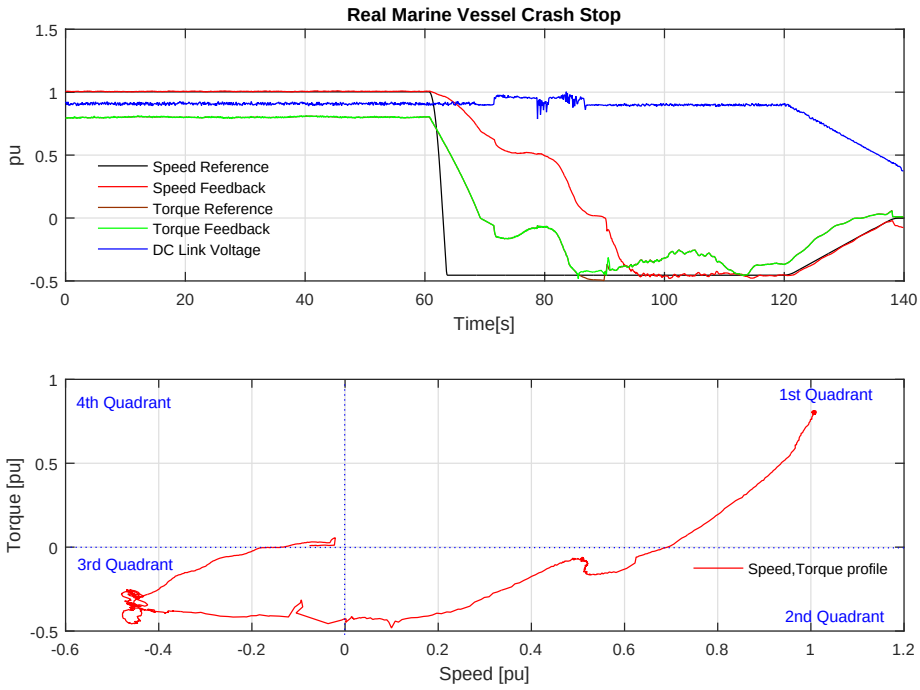

Fig. 9.33 Real Marine Vessel Crash Stop

Figure 9.34, figure 9.35 , figure 9.36 and figure 9.37 show the simulted and experimental measurement results for positive and negative speed crash stops taken on

the 24 phase electronically commutated dc machine laboratory prototype drive for a simulated crash stop where the load profile was modelled on the load drive as depicted in 9.31. Figure 9.34 shows the measured dc link voltage, electronic commutator and machine phase current and voltages during the crash stop. As can be seen the drive is capable of operating in all four quadrants. The simulation model gave similar results as shown in Figure 9.35 for the crash stop manoeuvre. In this topology, quadrant reversals is achieved through dc link voltage polarity reversal by the electronic commutator with dc link uni-directional current. For the positive uni-directional dc link current, the motoring quadrants are depicted by positive dc link voltages and the generating mode by negative dc link voltages.

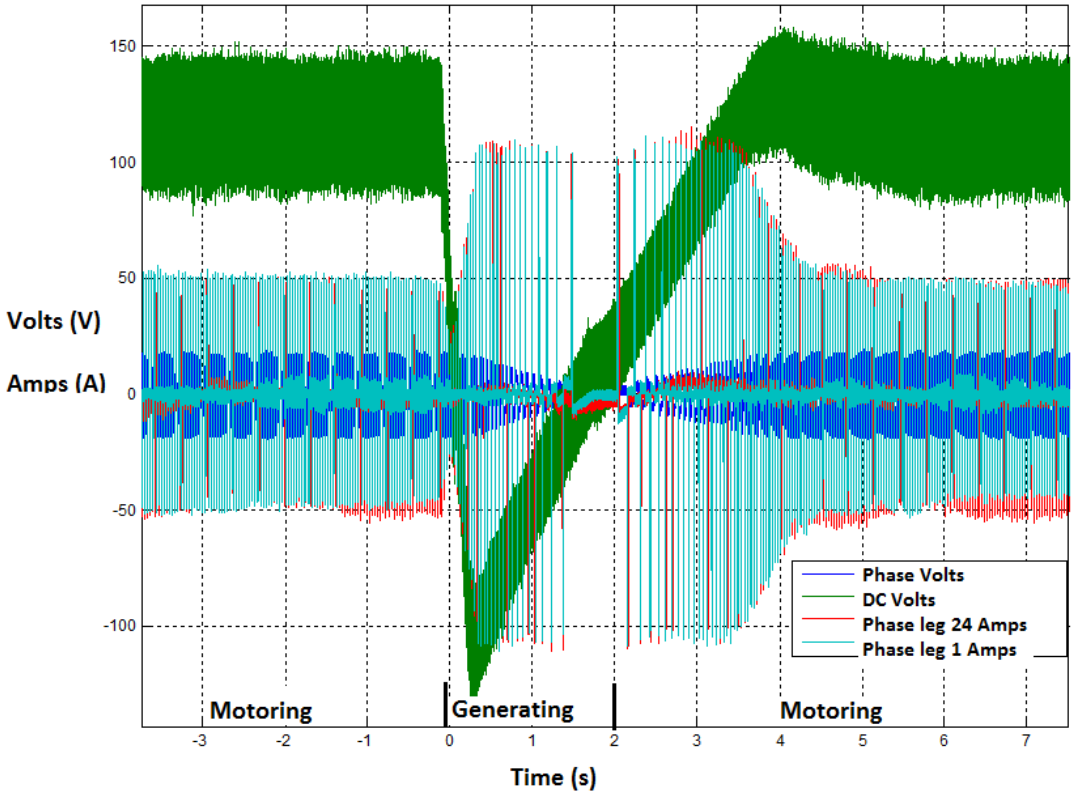

Fig. 9.34 Experimental Measurement: Crash Stop at 0.5pu speed, DC Voltage, Machine Phase Voltage & Electronic Commutator Voltage & Current Waveforms

Simulation Results

Simulation results also confirmed robust full four quadrant dynamic operation under worst case conditions where torque reversals and speed reversals occur at rated per unit values as depicted in figure 9.38. Figure 9.39 shows the corresponding dc link,

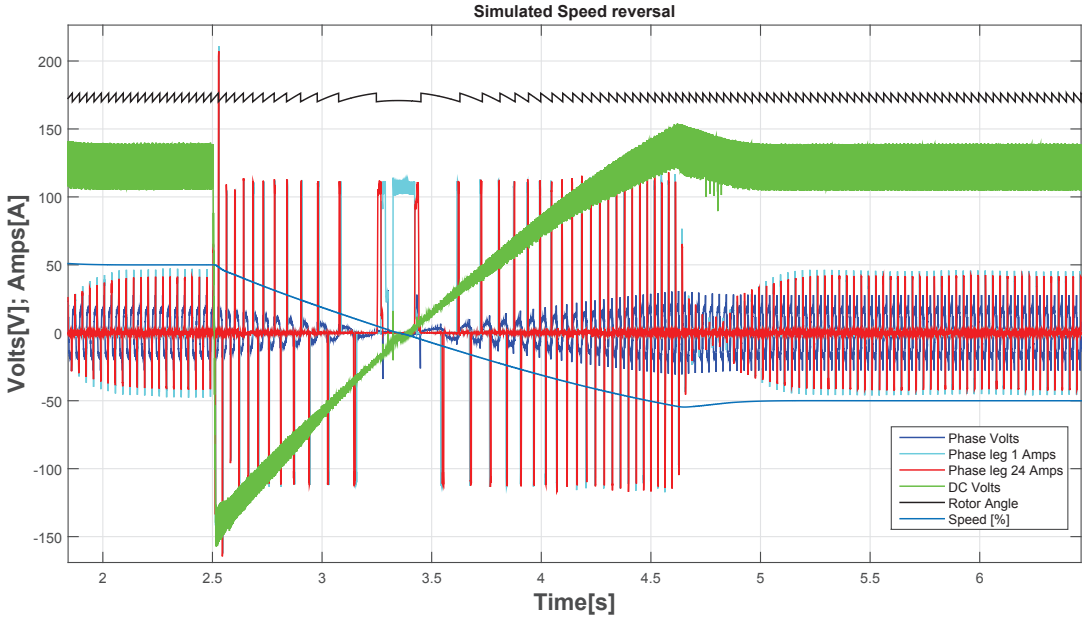

Fig. 9.35 Simulation Results: Crash Stop at 0.5pu Speed, DC Voltage, Machine Phase Voltage & Electronic Commutator Voltage & Current Waveforms

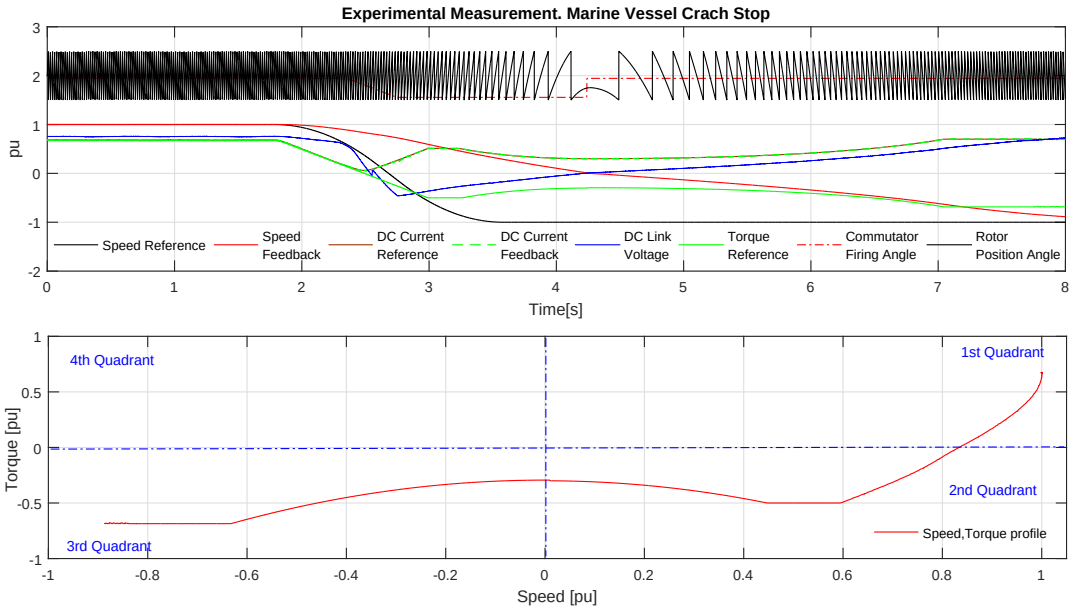

Fig. 9.36 Experimental Measurement: 1.0 pu Speed Vessel Crash Stop Astern

electronic commutator and machine voltages and currents. Current and voltage spikes can be seen near zero speed due to electronic commutator forced current commutation action. This is due to that fact that near zero speed there isn't sufficient machine phase voltage to cause natural current commutation and the electronic commutator has to

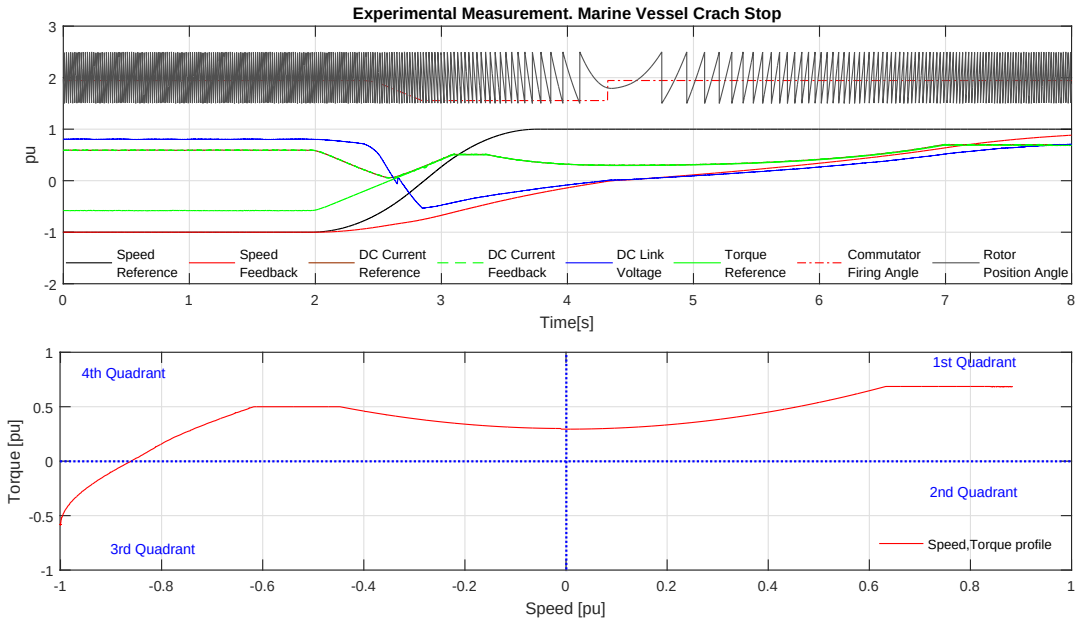

Fig. 9.37 Experimental Measurement: 1.0 pu Speed Vessel Crash Stop Ahead

be operated in forced commutation mode. Figure 9.40 shows a zoom of figure 9.39 around the zero speed transition zone.

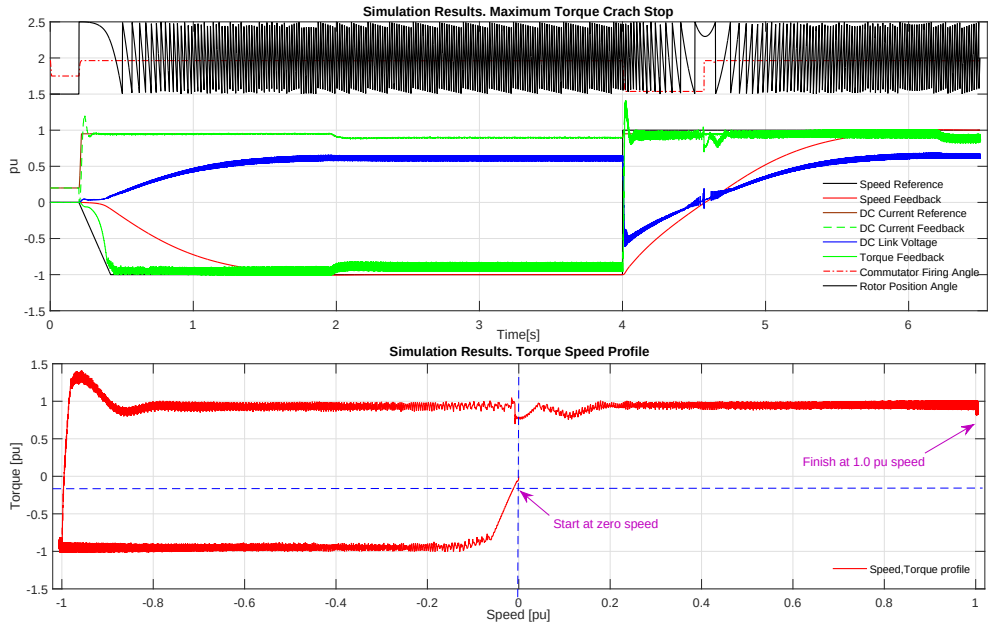

Fig. 9.38 Simulation: 1.0 pu Speed, 1.0 pu Torque Arduous Crash Stop Ahead

The crash stop experimental measurement and simulation results have demonstrated that the proposed control strategy for multiphase electronic commutated dc machines is viable and gives good transient, dynamic and steady state performance.

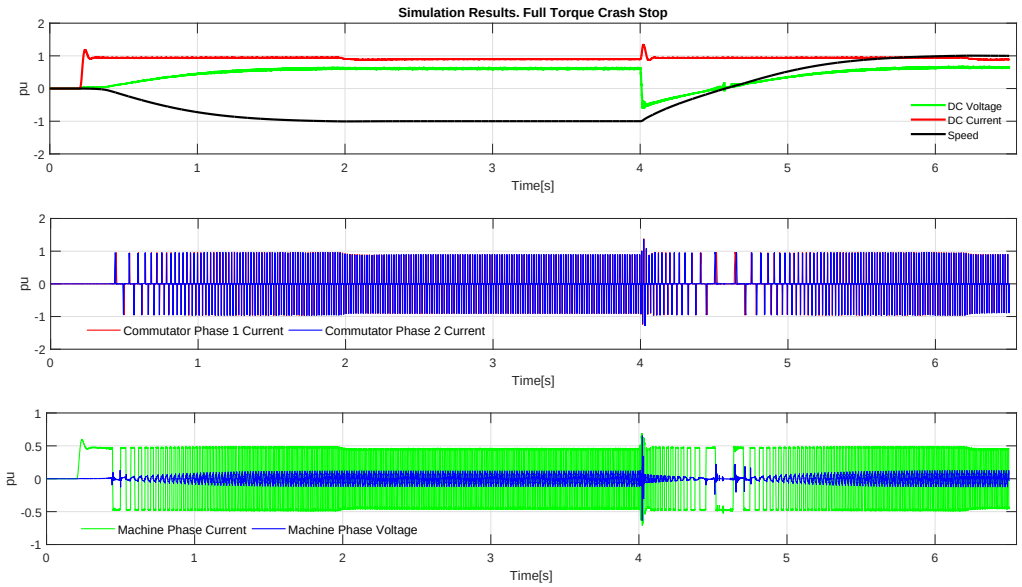

Fig. 9.39 Simulation: 1.0 pu Speed, 1.0 pu Crash Stop Machine Voltage and Currents

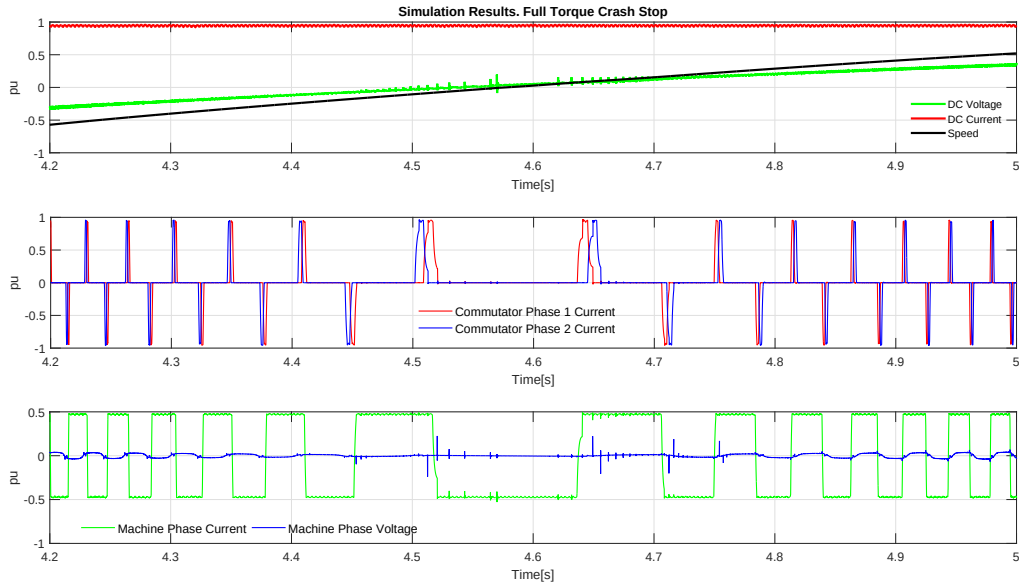

Fig. 9.40 Simulation: 1.0 pu Speed, 1.0 pu Crash Stop Machine Voltage and Currents Zoom at Speed Reversal

Successful four quadrant operation of the drive over the entire torque speed range has been demonstrated against an arduous marine propulsion drive crash stop duty. The simulation studies and experimental validation of both even and odd number of stator phase topologies have proved the viability of;

- the proposed electronic commutator control scheme,

- the natural and forced current commutation modes operation of the electronic commutator,
- the robust controllers for speed, dc link current, flux and field current control,
- the good dynamic and steady state operation,
- the full four quadrant operation over the entire drive torque speed range.

Simulation and experimental tests have shown that good performance and fault detection is achievable without the need for measuring individual machine or electronic commutator phase currents or voltages. Instead, only a balanced three phase set of machine differential voltages is necessary for control and the use of dc link current and clamp capacitor voltage measurement was deemed adequate for detection of machine and electronic commutator faults.

9.4 Discussion

Simulation studies and experimental measurements have shown that the electronic commutator can be controlled to exactly mimic the operation of the mechanical brushed commutator. In comparison to conventional machines, electronic commutation has been shown to be versatile as it allows full four quadrant operation for both even and odd phase numbered topologies. Furthermore, electronic commutation provides additional degrees of freedom by allowing natural, hybrid and forced current commutation modes which can be exploited to optimize the footprint and cost of the overall drive solution.

In both experimental prototype drives, no attempt was made at recovering the energy transferred to the auxiliary clamp circuits during current commutation, instead it was resistively dissipated as heat. Further improvements can be made to the design by employing energy recovery circuits to recover the energy back into the drive system.

Simulation and experimental results presented showed that electronic current commutation is inductively dominated, thus highlighted the need for ensuring balanced commutation and circuit loop inductances between all machine phases to ensure symmetrical duty on electronic commutator phase components and auxiliary clamp

circuit components. The use of auxiliary clamp capacitor voltage parity for internal machine and electronic commutator fault detection was seen to be effective.

Chapter 10

Conclusion and Future Work

The main research objectives of this work as setout in chapter 1 involved exploring alternative machine & power electronics converter topologies suitable for dc power system applications and developing appropriate simulation models & suitable control strategies for these proposed topologies. The final objective was to experimentally prove and demonstrate the viability of the proposed topologies and their associated control strategies. This work has been successful, experimental results have confirmed the viability of the proposed machine & converter topologies and demonstrated that the proposed control strategy delivers robust full four quadrant drive operation.

10.1 Conclusion

This work has presented, analysed and fully characterised the operational behaviour of multiphase electronically commutated dc machines. The work has demonstrated that this machine and converter topology is a viable machine and converter topology. The analysis and experimental tests have shown that indeed increasing the machine stator phase number to values significantly greater than three shifts the undesirable low order harmonics to higher orders where their impact on drive performance diminish with increasing phase number. This has been shown by analysis and experimental tests conducted on two multiphase electronically commutated dc machines, one with 15 stator phases and another with 24 stator phases.

The work has shown that both even and odd number of stator phase topologies are viable. Fully pitched concentric windings can be used with the even number

topologies. However, odd number topologies require short pitched winding functions to enable elimination of circulating currents. Comparative analysis of the even and odd number of stator phases presented in chapter 3 has shown that on balance, the benefits of odd-phase number topology in terms of cost, reliability and air gap torque ripple outweigh its drawbacks and is an attractive alternative proposition to the even numbered topology.

Electronic current commutation strategies for both even and odd number topologies have been presented and analysed and the key factors that influence the design and operation of the electronic commutator have been highlighted. The electronic current commutation process was seen to be inductively dominated and the machine commutating inductance and circuit loop inductance were seen to play a significant role. Incorporation of machine damper windings was experimentally proven to be effective at reducing the machine commutating inductance. However, the impact of the damper windings on overall machine performance such as on machine losses etc was not characterised. The scope was limited to assessing the impact on commutating inductance with a view to minimising its impact on the electronic commutator power electronics design. Experimental results also demonstrated that armature reaction plays a bigger role on the machine of this topology owing to the absence of commutating poles. This will have to be borne in mind when designing full scale machines to ensure armature reaction effects are fully accounted for and minimised as part of the machine design.

Since the multiphase electronically commutated dc machine topology departs from the conventional topologies, and requires closer integration of power electronics and machines, an alternative simulation modelling method that facilitates close integration of the machine and power electronics has been presented. Voltage behind reactance simulation models developed confirmed that power electronic converters can be easily interfaced to the machine model without compromising the stability of the simulations and without noticeable degradation in simulation time. The generic formulation of this model presented in this work makes it applicable to various machine converter topologies for detailed studies and characterisation of these drive systems. Further refinements will be required to accurately model the trapezoidal back emf, saturation effects and armature reaction effects.

Both simulation and experimental results from the two laboratory prototype drives have confirmed that the proposed electronic commutator and machine control strategy is viable and enables the drive to deliver full four quadrant operational performance. The control scheme formulation adopted has exposed the control parameters that enable independent control of dynamic reference signal tracking and plant noise disturbance rejection. It has also been shown that using the *MT*-axis reference frame coordinate systems enables the machine torque and flux control to be independently and selectively influenced. The results have shown that electronic commutator can cope with very high dynamic control requirements such as very fast torque changes. This has been demonstrated via simulated marine ship propulsion crash stop manoeuvre, which agrees with experiment.

This work has also practically demonstrated successfully the integration of power electronics into the machine stator housing using unencapsulated whole wafer power electronics devices with liquid dielectric cooling. Some of the factors that affect electromechanical integration were presented. Midel 7131 was successfully used as a liquid dielectric coolant owing to its very high dielectric strength which significantly reduced creepage and clearance distances, thus yielding compact electronic commutator design. One of the primary benefits of using Midel 7131 has been its ability to operate reliably at high temperatures over a sustained period of time. This in turn has facilitated more compact power electronic designs, and yielded considerable space savings that satisfied thermal design, insulation coordination and overall cost.

In summary, the research work has been successful, the proposed drive topologies and their control strategies have been analysed and experimentally validated as viable. Further research work will be required as outlined below.

10.2 Further Work

The work conducted has proven the viability of the proposed topology on laboratory scale prototypes. Further work is required to take this beyond the concept stage to full commercial exploitation. The simulation models developed in this work will require further enhancements to accurately model the machine saturation effects and machine armature reaction effects. In the control strategy presented in this work, no attempt was

made for full sensorless drive control, instead a combination of shaft speed sensor and stator voltage feedbacks were used for machine control to prove the concept. Further work is required to explore ways of developing full sensorless drive control strategies to enhance the robustness of the drive and minimise the use of sensors such as shaft encoders.

Concept stage integration of power electronics into the machine housing has shown promising results. Further work on integration of power electronics with machine will be required to further explore compact packaging, thermal management, mechanical vibration and electromagnetic compatibility issues. Furthermore, optimisation tools have to be developed to enable the right tradeoffs on design parameters that affect the machine and the power electronics design with respect to efficiency improvements and overall footprint reduction.

Although analytical work has been presented on the multilevel topology, it has not been possible to experimentally validate this topology due to time and financial constraints. Further work is required to experimentally prove this concept for high voltage dc applications.

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Appendix A

Machine Modelling

The Block matrices for the derivative equations of the rotor *qd* currents referred to in equation eqn(5.21) are given below.

The block matrix **A** is given by:

$$\mathbf{A} = \left[\begin{array}{cccc|cccc} -\frac{r_{kq1}}{L_{kq1}^2} & -\frac{r_{kq2}}{L_{kq2}^2} & \cdots & -\frac{r_{kqn}}{L_{kqn}^2} & 0 & 0 & \cdots & 0_n \\ 0 & 0 & \cdots & 0_m & 0 & \frac{-r_{kd1}}{L_{kd1}^2} & \cdots & \frac{-r_{kdm}}{L_{kdm}^2} \end{array}\right] \tag{A.1}$$

The block matrix **B** is given by:

$$\mathbf{B} = \left[\begin{array}{c|c} \overset{\mathbf{B_q}}{-(\frac{r_{kq1}}{L_{kq1}^2} + \frac{r_{kq2}}{L_{kq2}^2} + \cdots)} & \overset{\mathbf{B_d}}{0} \\ 0 & -(\frac{r_{kd1}}{L_{kd1}^2} + \frac{r_{kd2}}{L_{kd2}^2} + \cdots) \end{array}\right] \tag{A.2}$$

The block matrix **C** is given by:

$$\mathbf{C} = \left[\begin{array}{c|c} (\frac{1}{L_{kq1}} + \frac{1}{L_{kq2}} + \cdots) & 0 \\ 0 & (\frac{1}{L_{kd1}} + \frac{1}{L_{kd2}} + \cdots) \end{array}\right] \tag{A.3}$$

The matrix **D** is given by:

$$\mathbf{D} = \left[\begin{array}{c} 0 \\ -1 \end{array}\right] \tag{A.4}$$

The block matrix **E** is given by:

$$\mathbf{E} = \left[\begin{array}{cc} L_{kq1} & 0 \\ 0 & 0 \\ \vdots & \vdots \\ 0_n & 0_n \\ \hline 0 & 0 \\ 0 & L_{kd1} \\ 0 & 0 \\ \vdots & \vdots \\ 0_m & 0_m \end{array}\right] \tag{A.5}$$

The block matrices for the internal rotor network state vectors y_{qd} given in equation (5.57) are given below.

The block matrix $\mathbf{F}$ is given by:

$$\mathbf{F} = \left[\begin{array}{c} 0 \\ \vdots \\ 0_n \\ \hline -L_{fd} \\ L_{kd1} \\ \vdots \\ 0_m \end{array}\right] \tag{A.6}$$

The block matrix $\mathbf{G}$ is given by:

$$\mathbf{G} = \left[\begin{array}{c} (\frac{-L_{kq1}}{L''_{mq}}\lambda_{mq} - L_{kq1}(\frac{y_{q2}}{L_{kq2}} + \frac{y_{q3}}{L_{kq3}} + \cdots) \\ y_{q1} \\ \vdots \\ y_{qn} \\ \hline -\lambda_{md} \\ -L_{kd1}(\frac{\lambda_{md}}{L''_{md}} - \frac{\lambda_{md}}{L_{fd}} + \frac{y_{d3}}{L_{kd_2}} + \frac{y_{d4}}{L_{kd_3}} + \cdots) \\ y_{d3} \\ \vdots \\ y_{dm} \end{array}\right] \tag{A.7}$$

The matrix $\mathbf{H}$ in the field voltage equation (5.11) is given as:

$$\mathbf{H} = \left[\begin{array}{cccc} \frac{-r_{fd}}{L_{fd}} & 0 & 0 & \cdots \end{array}\right] \tag{A.8}$$

Appendix B

Experimental Prototypes Drives Design

Tables B.1, B.2 and B.3 shows the SHE PWM state machine states and the corresponding CSR switching devices S_1 to S_7 conduction states. A zero signified a device thats switched OFF and a 1 signifies a device thats switched ON.

Tables B.4 and B.5 show the computed chopping angles for the entire SHE modulation range. A modulation resolution of 1% was deemed sufficient and used to compute the chopping angles.

Fig. B.1 SHE PWM Converter State Machine Sector 1 & 2: Device S_1 to S_7 States

Sector	state	S1	S2	S3	S4	S5	S6	S7
0	1	1	0	0	0	1	0	0
	2	1	0	0	0	0	1	0
	3	1	0	0	1	0	0	1
	4	1	0	0	0	1	0	0
	5	1	0	0	0	0	1	0
	6	1	0	0	1	0	0	1
	7	1	0	0	0	1	0	0
	8	1	0	0	0	0	1	0
	9	1	0	0	0	1	0	0
	10	1	0	0	0	0	1	0
	11	1	0	0	1	0	0	1
	12	1	0	0	0	1	0	0
	13	1	0	0	0	0	1	0
	14	1	0	0	1	0	0	1
	15	1	0	0	0	1	0	0
	16	1	0	0	0	0	1	0

Sector	state	S1	S2	S3	S4	S5	S6	S7
1	17	1	0	0	0	0	1	0
	18	0	1	0	0	0	1	0
	19	0	0	1	0	0	1	1
	20	1	0	0	0	0	1	0
	21	0	1	0	0	0	1	0
	22	0	0	1	0	0	1	1
	23	1	0	0	0	0	1	0
	24	0	1	0	0	0	1	0
	25	1	0	0	0	0	1	0
	26	0	1	0	0	0	1	0
	27	0	0	1	0	0	1	1
	28	1	0	0	0	0	1	0
	29	0	1	0	0	0	1	0
	30	0	0	1	0	0	1	1
	31	1	0	0	0	0	1	0
	32	0	1	0	0	0	1	0

Fig. B.2 SHE PWM Converter State Machine Sector 3 & 4: Device S_1 to S_7 States

Sector	state	S1	S2	S3	S4	S5	S6	S7
2	33	0	1	0	0	0	1	0
	34	0	1	0	1	0	0	0
	35	0	1	0	0	1	0	1
	36	0	1	0	0	0	1	0
	37	0	1	0	1	0	0	0
	38	0	1	0	0	1	0	1
	39	0	1	0	0	0	1	0
	40	0	1	0	1	0	0	0
	41	0	1	0	0	0	1	0
	42	0	1	0	1	0	0	0
	43	0	1	0	0	1	0	1
	44	0	1	0	0	0	1	0
	45	0	1	0	1	0	0	0
	46	0	1	0	0	1	0	1
	47	0	1	0	0	0	1	0
	48	0	1	0	1	0	0	0

Sector	state	S1	S2	S3	S4	S5	S6	S7
3	49	0	1	0	1	0	0	0
	50	0	0	1	1	0	0	0
	51	1	0	0	1	0	0	1
	52	0	1	0	1	0	0	0
	53	0	0	1	1	0	0	0
	54	1	0	0	1	0	0	1
	55	0	1	0	1	0	0	0
	56	0	0	1	1	0	0	0
	57	0	1	0	1	0	0	0
	58	0	0	1	1	0	0	0
	59	1	0	0	1	0	0	1
	60	0	1	0	1	0	0	0
	61	0	0	1	1	0	0	0
	62	1	0	0	1	0	0	1
	63	0	1	0	1	0	0	0
	64	0	0	1	1	0	0	0

Fig. B.3 SHE PWM Converter State Machine Sector 5 & 6: Device S_1 to S_7 States and Trip State

Sector	state	S1	S2	S3	S4	S5	S6	S7
4	65	0	0	1	1	0	0	0
	66	0	0	1	0	1	0	0
	67	0	0	1	0	0	1	1
	68	0	0	1	1	0	0	0
	69	0	0	1	0	1	0	0
	70	0	0	1	0	0	1	1
	71	0	0	1	1	0	0	0
	72	0	0	1	0	1	0	0
	73	0	0	1	1	0	0	0
	74	0	0	1	0	1	0	0
	75	0	0	1	0	0	1	1
	76	0	0	1	1	0	0	0
	77	0	0	1	0	1	0	0
	78	0	0	1	0	0	1	1
	79	0	0	1	1	0	0	0
	80	0	0	1	0	1	0	0

Sector	state	S1	S2	S3	S4	S5	S6	S7
5	81	0	0	1	0	1	0	0
	82	1	0	0	0	1	0	0
	83	0	1	0	0	1	0	1
	84	0	0	1	0	1	0	0
	85	1	0	0	0	1	0	0
	86	0	1	0	0	1	0	1
	87	0	0	1	0	1	0	0
	88	1	0	0	0	1	0	0
	89	0	0	1	0	1	0	0
	90	1	0	0	0	1	0	0
	91	0	1	0	0	1	0	1
	92	0	0	1	0	1	0	0
	93	1	0	0	0	1	0	0
	94	0	1	0	0	1	0	1
	95	0	0	1	0	1	0	0
	96	1	0	0	0	1	0	0

Trip State	0	0	0	0	0	0	0	1

Fig. B.4 SHE PWM Table of Switching Angles Against Modulation for 7 Switching Angles for 0.01 to 0.6pu Modulation

Modulation	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09	0.1
theta1	0.0009796	0.0019597	0.0029402	0.0039211	0.0049024	0.0058839	0.0068657	0.0078477	0.0088299	0.0098123
theta2	0.001287	0.0025724	0.003856	0.005138	0.0064183	0.007697	0.0089741	0.01025	0.011524	0.012796
theta3	0.26061	0.25941	0.25822	0.25703	0.25583	0.25464	0.25344	0.25225	0.25105	0.24985
theta4	0.26246	0.26311	0.26377	0.26442	0.26507	0.26572	0.26637	0.26702	0.26766	0.2683
theta5	0.26313	0.26447	0.2658	0.26713	0.26846	0.26979	0.27111	0.27244	0.27376	0.27508
theta6	0.52229	0.52098	0.51967	0.51837	0.51706	0.51576	0.51445	0.51315	0.51184	0.51054
theta7	0.5231	0.52261	0.52212	0.52163	0.52115	0.52068	0.5202	0.51974	0.51928	0.51882

Modulation	0.11	0.12	0.13	0.14	0.15	0.16	0.17	0.18	0.19	0.2
theta1	0.010795	0.011777	0.01276	0.013742	0.014724	0.015707	0.016689	0.017671	0.018653	0.019634
theta2	0.014067	0.015336	0.016604	0.017871	0.019136	0.020399	0.021661	0.022922	0.024181	0.025439
theta3	0.24866	0.24746	0.24626	0.24507	0.24387	0.24267	0.24147	0.24027	0.23907	0.23787
theta4	0.26894	0.26958	0.27022	0.27085	0.27148	0.27211	0.27274	0.27336	0.27398	0.2746
theta5	0.2764	0.27772	0.27903	0.28035	0.28166	0.28298	0.28429	0.2856	0.28691	0.28821
theta6	0.50924	0.50793	0.50663	0.50533	0.50403	0.50273	0.50143	0.50013	0.49883	0.49753
theta7	0.51837	0.51792	0.51748	0.51705	0.51662	0.51619	0.51577	0.51535	0.51494	0.51454

Modulation	0.21	0.22	0.23	0.24	0.25	0.26	0.27	0.28	0.29	0.3
theta1	0.020615	0.021596	0.022576	0.023556	0.024536	0.025515	0.026493	0.027471	0.028449	0.029425
theta2	0.026695	0.02795	0.029203	0.030456	0.031706	0.032956	0.034204	0.03545	0.036695	0.037939
theta3	0.23667	0.23547	0.23427	0.23307	0.23187	0.23067	0.22947	0.22826	0.22706	0.22586
theta4	0.27521	0.27582	0.27643	0.27704	0.27764	0.27824	0.27884	0.27943	0.28002	0.28061
theta5	0.28952	0.29083	0.29213	0.29343	0.29473	0.29603	0.29733	0.29863	0.29993	0.30122
theta6	0.49623	0.49493	0.49363	0.49233	0.49103	0.48973	0.48844	0.48714	0.48584	0.48454
theta7	0.51414	0.51375	0.51336	0.51298	0.51261	0.51224	0.51187	0.51151	0.51116	0.51082

Modulation	0.31	0.32	0.33	0.34	0.35	0.36	0.37	0.38	0.39	0.4
theta1	0.030401	0.031376	0.032351	0.033324	0.034297	0.035268	0.036239	0.037208	0.038177	0.039144
theta2	0.039181	0.040422	0.041662	0.0429	0.044137	0.045372	0.046606	0.047839	0.049069	0.050299
theta3	0.22465	0.22345	0.22224	0.22104	0.21983	0.21862	0.21742	0.21621	0.215	0.21379
theta4	0.28119	0.28177	0.28234	0.28291	0.28348	0.28404	0.2846	0.28516	0.28571	0.28625
theta5	0.30252	0.30381	0.3051	0.30639	0.30768	0.30897	0.31026	0.31155	0.31283	0.31412
theta6	0.48324	0.48194	0.48065	0.47935	0.47805	0.47675	0.47545	0.47415	0.47285	0.47155
theta7	0.51048	0.51015	0.50982	0.5095	0.50919	0.50888	0.50858	0.50828	0.508	0.50772

Modulation	0.41	0.42	0.43	0.44	0.45	0.46	0.47	0.48	0.49	0.5
theta1	0.04011	0.041075	0.042039	0.043001	0.043962	0.044921	0.045879	0.046835	0.04779	0.048742
theta2	0.051527	0.052753	0.053978	0.055202	0.056424	0.057644	0.058862	0.060079	0.061294	0.062508
theta3	0.21258	0.21137	0.21016	0.20895	0.20773	0.20652	0.2053	0.20409	0.20287	0.20166
theta4	0.2868	0.28733	0.28787	0.2884	0.28892	0.28944	0.28995	0.29046	0.29097	0.29147
theta5	0.3154	0.31668	0.31796	0.31924	0.32052	0.3218	0.32307	0.32434	0.32562	0.32689
theta6	0.47025	0.46895	0.46765	0.46635	0.46505	0.46375	0.46245	0.46114	0.45984	0.45854
theta7	0.50744	0.50718	0.50692	0.50666	0.50642	0.50618	0.50595	0.50572	0.50551	0.5053

Modulation	0.51	0.52	0.53	0.54	0.55	0.56	0.57	0.58	0.59	0.6
theta1	0.049693	0.050642	0.051589	0.052534	0.053476	0.054417	0.055355	0.056291	0.057224	0.058154
theta2	0.06372	0.064929	0.066137	0.067343	0.068547	0.069749	0.070949	0.072147	0.073342	0.074535
theta3	0.20044	0.19922	0.198	0.19678	0.19555	0.19433	0.1931	0.19188	0.19065	0.18942
theta4	0.29196	0.29245	0.29293	0.29341	0.29388	0.29435	0.29481	0.29527	0.29572	0.29616
theta5	0.32816	0.32943	0.33069	0.33196	0.33322	0.33449	0.33575	0.33701	0.33826	0.33952
theta6	0.45723	0.45592	0.45462	0.45331	0.452	0.45069	0.44938	0.44807	0.44675	0.44544
theta7	0.50509	0.5049	0.50471	0.50453	0.50435	0.50419	0.50403	0.50387	0.50373	0.50359

Fig. B.5 SHE PWM Table of Switching Angles Against Modulation for 7 Switching Angles for 0.61 to 0.98pu Modulation

Modulation	0.61	0.62	0.63	0.64	0.65	0.66	0.67	0.68	0.69	0.7
theta1	0.059081	0.060006	0.060927	0.061846	0.06276	0.063672	0.064579	0.065483	0.066382	0.067277
theta2	0.075726	0.076914	0.078099	0.079282	0.080461	0.081638	0.082811	0.083981	0.085148	0.08631
theta3	0.18818	0.18695	0.18571	0.18448	0.18324	0.18199	0.18075	0.1795	0.17825	0.177
theta4	0.2966	0.29703	0.29745	0.29787	0.29828	0.29868	0.29908	0.29947	0.29986	0.30023
theta5	0.34077	0.34202	0.34327	0.34451	0.34576	0.347	0.34824	0.34947	0.3507	0.35193
theta6	0.44412	0.4428	0.44148	0.44016	0.43883	0.4375	0.43617	0.43484	0.4335	0.43216
theta7	0.50346	0.50333	0.50321	0.5031	0.50299	0.50289	0.50279	0.5027	0.50261	0.50253

Modulation	0.71	0.72	0.73	0.74	0.75	0.76	0.77	0.78	0.79	0.8
theta1	0.068167	0.069052	0.069932	0.070807	0.071679	0.072541	0.073397	0.074245	0.075086	0.075918
theta2	0.087469	0.088623	0.089772	0.090917	0.092059	0.093193	0.094321	0.095443	0.096557	0.097663
theta3	0.17574	0.17448	0.17321	0.17194	0.17067	0.16939	0.16811	0.16682	0.16552	0.16422
theta4	0.3006	0.30096	0.30131	0.30165	0.30199	0.30232	0.30263	0.30294	0.30323	0.30352
theta5	0.35315	0.35437	0.35558	0.35679	0.358	0.35919	0.36038	0.36156	0.36273	0.36389
theta6	0.43082	0.42947	0.42811	0.42675	0.42539	0.42402	0.42264	0.42126	0.41986	0.41845
theta7	0.50245	0.50237	0.5023	0.50222	0.50215	0.50207	0.50198	0.5019	0.5018	0.50169

Modulation	0.81	0.82	0.83	0.84	0.85	0.86	0.87	0.88	0.89	0.9
theta1	0.076742	0.077555	0.078357	0.079148	0.079926	0.080689	0.081436	0.082165	0.082873	0.083558
theta2	0.098761	0.099849	0.10093	0.10199	0.10305	0.10409	0.10511	0.10611	0.10709	0.10805
theta3	0.1629	0.16158	0.16025	0.15891	0.15755	0.15618	0.1548	0.15339	0.15197	0.15051
theta4	0.30379	0.30405	0.30429	0.30452	0.30473	0.30492	0.30509	0.30523	0.30534	0.30541
theta5	0.36504	0.36618	0.36729	0.36839	0.36947	0.37052	0.37154	0.37252	0.37345	0.37432
theta6	0.41704	0.4156	0.41416	0.41269	0.4112	0.40968	0.40813	0.40654	0.40491	0.40321
theta7	0.50157	0.50143	0.50126	0.50107	0.50084	0.50056	0.50022	0.49982	0.49932	0.4987

Modulation	0.91	0.92	0.93	0.94	0.95	0.96	0.97	0.98
theta1	0.084215	0.08484	0.085425	0.085962	0.086437	0.086825	0.087085	0.087121
theta2	0.10897	0.10986	0.11069	0.11147	0.11216	0.11273	0.1131	0.11311
theta3	0.14903	0.1475	0.14593	0.1443	0.14258	0.14073	0.13868	0.13625
theta4	0.30544	0.3054	0.30528	0.30505	0.30466	0.304	0.30287	0.30083
theta5	0.37511	0.37579	0.37632	0.37664	0.37665	0.37615	0.37479	0.37174
theta6	0.40143	0.39954	0.3975	0.39526	0.3927	0.38965	0.38574	0.38016
theta7	0.49794	0.49699	0.49578	0.49423	0.4922	0.48945	0.48557	0.47974

Appendix C

Machine Phase Number Comparison: Commutator Losses

C.1 Machine and Electronic Commutator Ratings

This appendix gives a summary of the electronic commutator losses calculation and device data sheets used in the comparison of 15 phase and 24 phase machines presented in chapter 3. In the phase number comparison, the following assumptions were made for the machine designs: (a) both machines have the same rated shaft power, (b) both machines have the same machine dimensions; (c) both machines have the same number of coil turns, (d) both machines have same rated shaft speed. This resulted in the ratings presented in table C.1 and table C.2 , which were used for the electronic commutator designs.

C.1.1 Machine Ratings

Table C.1 gives a summary of the 15 & 24 phase machine data used in the simulations.

C.1.2 Electronic Commutator Ratings

Table C.2 gives a summary of the 15 & 24 electronic commutator data used in the simulations.

C.1.3 Electronic Commutator Voltage Clamping Circuit

As discussed in chapter 3, the aim of the clamp circuit is to limit the voltage across the GTOs during forced turn-off commutations. The clamp circuit consists of clamp diodes (connected across each GTO), clamp capacitors and clamp discharge resistors. With reference to figure C.2, when the outgoing GTO is gated-off, its current decreases

Table C.1 Machine Parameters

	Parameter	Value	Unit
1	Shaft Speed	200	RPM
2	Number of Poles	6	
3	Stator Winding mean radius	0.645	m
4	Stator active length	0.560	m
5	Armature flux density	1.092	T
6	Number of turns per coil	2	
7	End winding voltage coefficient	1.07	
8	Coil resistance	10	$\mu\Omega$
	Parameter	**24 Phase**	**15 Phase**
9	Number of slots per pole pair	24	30
10	Number of phases	24	15
11	DC link Current	2400 A	1926 A
12	Commutating Inductance	10 μ H	40 μ H

Table C.2 24 Phase and 15 Phase Electronic Commutator Ratings

	24 Phase Machine	**15 Phase Machine**
Power (MW)	1.900	1.900
DC Voltage (V)	794 V	990 V
DC Current (A)	2400 A	1926 A
Phase Voltage (V)	100 V peak	200 V peak

very quickly with a di/dt which is mainly dependant on the GTO gatecard and the GTO itself. Because of the very high di/dt and commutating inductance, the clamp diode turns on nearly instantaneously. As current flows through the clamp diode, it charges the clamp capacitor up. The di/dt of the ingoing force commutated GTO current is governed by the ratio of the clamp voltage over the commutating inductance. The clamp diode current is the difference between the DC link current, the outgoing GTO current and the ingoing GTO current. When the diode current reaches zero, the clamp capacitor discharges into the clamp discharge resistor with a time constant dependant on the clamp discharge resistance and clamp capacitance.

The parameters used in the Mathcad simulation for the machine phase comparisons are given in table C.3. In the simulations, the clamp discharge capacitance and discharge resistance were set so that the mean clamp voltage was approximately 1500 V for both 15-phase and 24-phase configurations. The GTO data is based on ABB GTO SGA 15F2502 (asymmetric GTO, V_{DRM}= 2500 V, I_{TGQM} = 1500 A) and the clamp diode data is based on ABB 5SDD08D500 (rectifier diode,V_{RSM} = 5200 V, I_{FAVM} = 1028 A)

Figure C.1 shows the model parameters used in the thermal model.

Table C.3 Clamp Circuit Simulation Model Parameters

	Parameter	Value	Unit
1	GTO Turn-off di/dt	-600	A/μs
2	GTO natural commutated current	0.5	per unit
3	GTO tail current duration	15	μs
4	GTO tail current	0.1	per unit of forced commutation current
5	Fundamental frequency	10	Hz
	Parameter	**24 Phase**	**15 Phase**
6	Phase number	24	15
7	Commutating Inductance	10 μH	40 μH
8	DC Current	2400 A	1926 A
9	Clamp Capacitance	100 μF	150 μF
10	Clamp discharge resistance	2000 Ω	890 Ω

Fig. C.1 Thermal Simulation Model Parameters

Row	Parameter	Value	Unit
1	Nominal electrical frequency	10	Hz
2	GTO forward voltage drop	$V_{fwd}(i) = A + B \cdot i + C \cdot \ln(1+i) + D \cdot \sqrt{i}$ A = 11.7 10^{-3} B = 630.8 10^{-6} C = 340.2 10^{-3} D = -22.0 10^{-3}	V
3	Transient junction-to-case thermal impedance	$Z_{th\_jc}(t) = \frac{1}{1000} \cdot \sum_{i=1}^{4} \left[R_{thi} \cdot \left(1 - e^{\left(\frac{-t}{\tau_{thi}} \right)} \right) \right]$ $R_{th1} = 14.570$ $\tau_{th1} = 0.4610$ $R_{th1} = 5.051$ $\tau_{th1} = 0.0950$ $R_{th1} = 7.285$ $\tau_{th1} = 0.0120$ $R_{th1} = 0.097$ $\tau_{th1} = 0.0010$	ºC/W
4	Thermal resistance heatsink to case	0.008	ºC/W
5	Thermal resistance case to junction	0.027	ºC/W
6	Heatsink temperature	80	ºC
7	Force commutated current	0.5	Per unit of operating DC link current
8	Operating DC link current	Variable	Per unit of rated DC link current
9	Operating machine speed	Variable	Per unit of rated machine speed

Row	Parameter	24-phase		15-phase	
		Value	Unit	Value	Unit
10	Phase number	24	-	15	–
11	Commutating inductance	10	µH	40	µH
12	Rated DC link current	2411	A	1926	A
13	GTO turn-off energy [J]	$E_{off}(i_{pu}) = 6.99 \cdot i_{pu}^3 + 2.87 \cdot i_{pu}^2 - 0.03 \cdot i_{pu}$		$E_{off}(i_{pu}) = 4.59 \cdot i_{pu}^3 + 2.17 \cdot i_{pu}^2 - 0.0023 \cdot i_{pu}$	

C.1.4 GTO Conduction & Switching Losses Model

The power dissipated in the GTO is due to: (a) the conduction losses and (b) the switching losses (turn-on and turn-off). The turn-on losses are very low compared to the turn-off losses, so in the comparison presented they have been neglected. A Mathcad model was implemented to estimate the power dissipated in the GTOs for both 15-phase and 24-phase machines. The simulation model assumes that the GTOs turn off into a constant voltage equal to the mean clamp voltage. The figure C.2, figure C.3 and figure C.1 show the parameters used in the Mathcad model for the power loss comparison.

Fig. C.2 Mathcad Model Used for GTO Power Dissipation

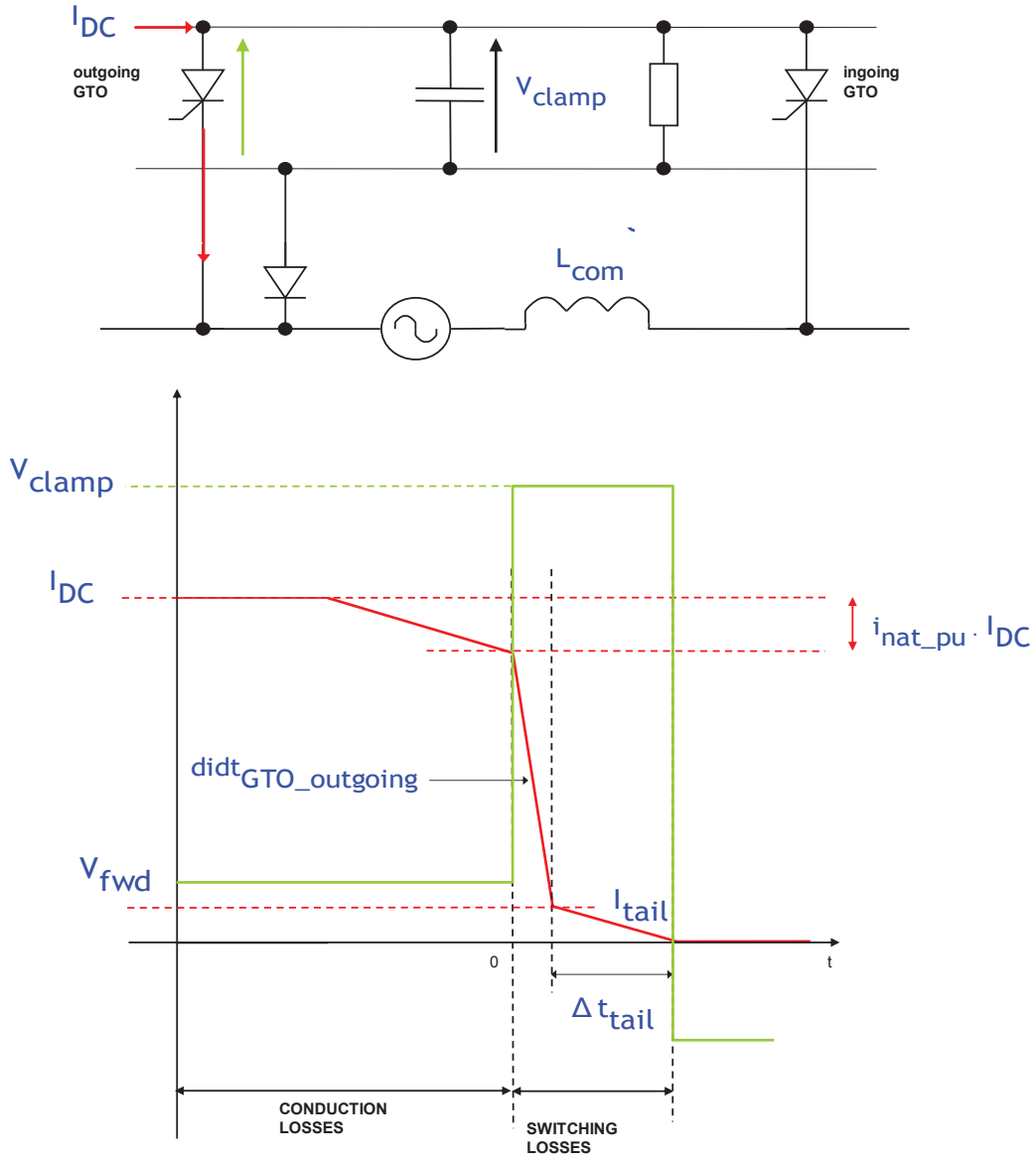
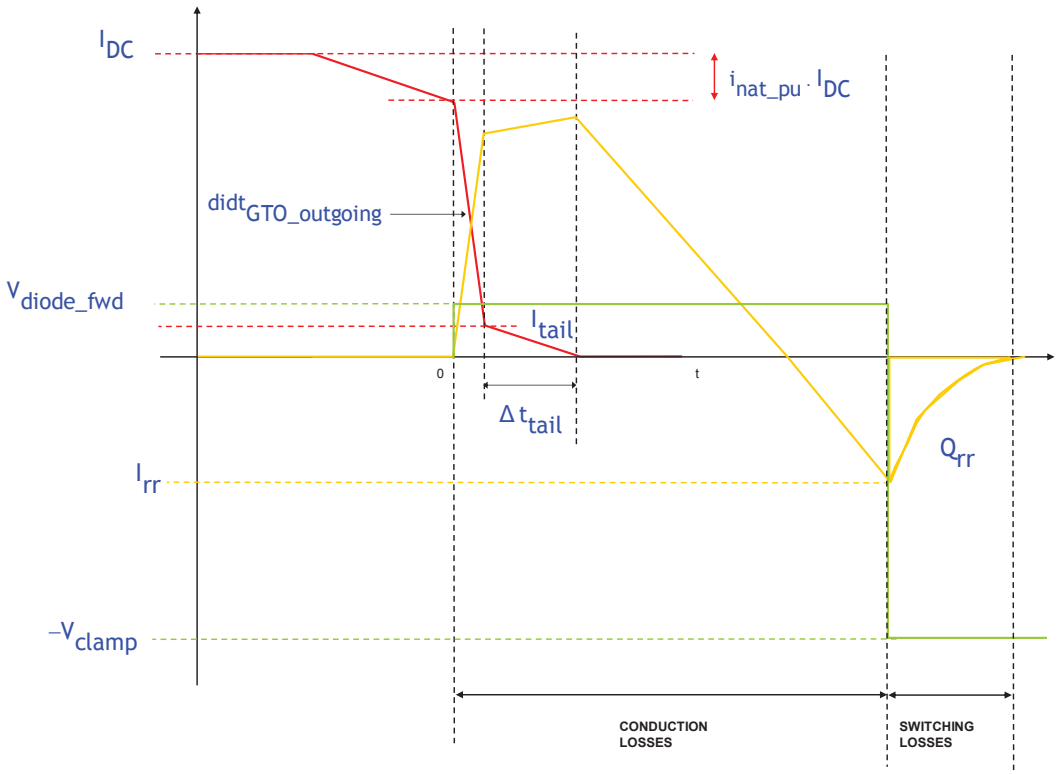


Fig. C.3 Mathcad Model Used for Clamp Diode Power Dissipation

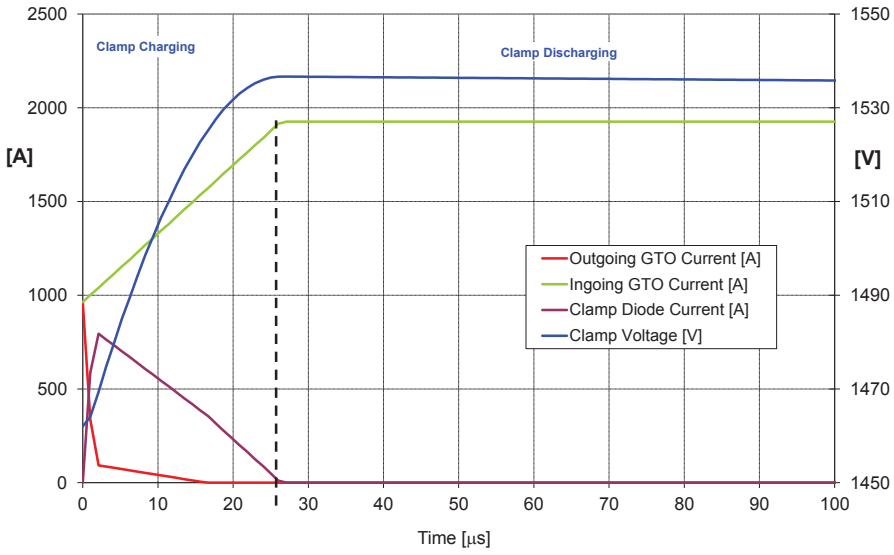


The simulated waveforms for 15 and 24 phase machines current commutator losses are given in figure C.4 , figure C.6, figure C.7 , figure C.5, figure C.8, figure C.9 and figure C.10.

C.1.5 Clamp Diode Losses Model

The power dissipated in the clamp diodes is due to: (a) the reverse recovery losses and (b) the conduction losses. The same Mathcad model as for the GTO power dissipation calculations was implemented to estimate the power dissipated in the clamp diodes for both 15-phase and 24-phase machines . The input data required for running the model is listed in table C.1, table C.2, table C.3 and figure C.1. The following assumptions are used in the model: (a) the clamp diode turns off into a constant voltage equal to negative clamp voltage -V_{clamp} and (b) the reverse recovery current is modelled by a decaying exponential function whose time constant is dependant on the maximum recovery current and the reverse recovery charge as illustrated in figure C.3. Figure C.9 and figure C.10 show the simulated device power losses for the 15 phase and 24 phase designs.

Fig. C.4 Simulated Clamp Circuit Switching Voltages and Currents



C.1.6 GTO Thermal Rating

A Mathcad model implemented to estimate the instantaneous GTO junction temperature for both 15-phase and 24-phase machines in steady-state is based on the following assumptions:

(a) The mean junction temperature of the GTO is calculated from the mean power dissipated in the GTO due to the conduction losses and turn-off switching losses, and the steady-state thermal resistances of the GTO (heatsink-to-case, case-to-junction). The mean GTO conduction losses are calculated from the operating DC link current, the GTO forward voltage drop and the number of phases. The mean GTO turn-off switching losses are calculated from the force commutated current, the operating mean clamp voltage (assumed to be proportional to the force commutated current) and the operating electrical frequency.

(b) The instantaneous junction temperature rise of the GTO is calculated from the instantaneous pulse of power dissipated in the GTO during the conduction time and the transient thermal case-to-junction impedance of the GTO. The instantaneous GTO turn-off energy is neglected for the calculations of the instantaneous junction temperature as the amount of energy dissipated is significantly less than the conduction losses and the energy is dissipated in a very short period of time (couple of μs).

(c) The heatsink temperature is assumed to be constant in steady-state.

Fig. C.5 Simulated Clamp Circuit Auxiliary DC Clamp Voltages

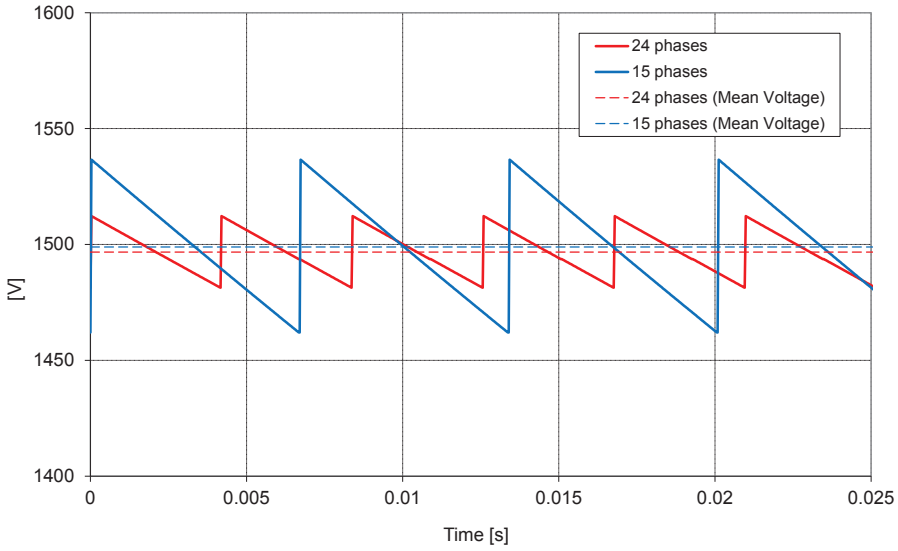


Fig. C.6 Simulated Junction Temperatures for 15 & 24 Phase Commutator Devices

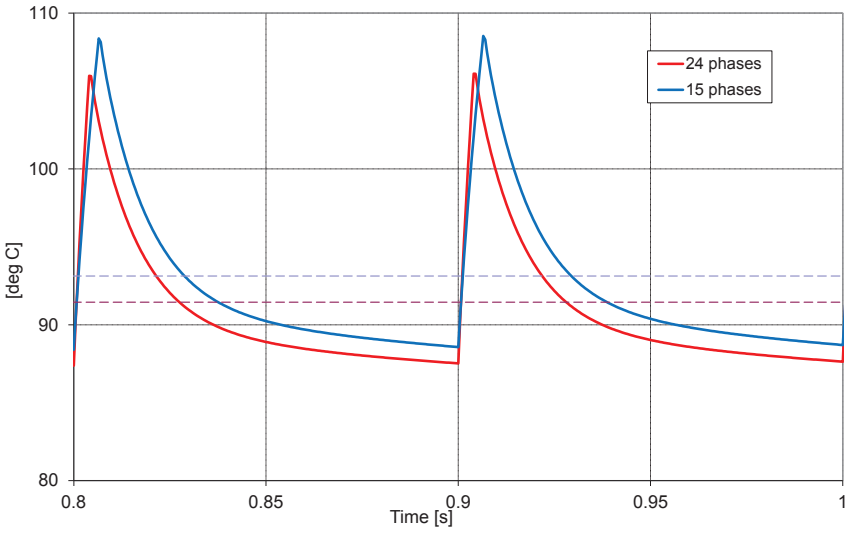


Fig. C.7 Simulated Device Power Dissipation for 24 Phase Commutator Devices Voltages & Currents

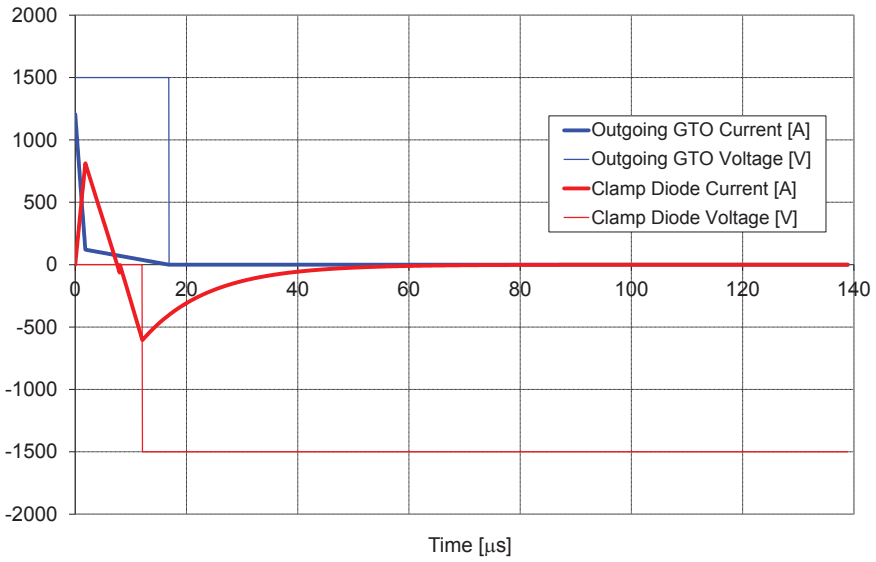


Fig. C.8 Simulated Device Power Dissipation for 15 Phase Commutator Devices Voltages & Currents

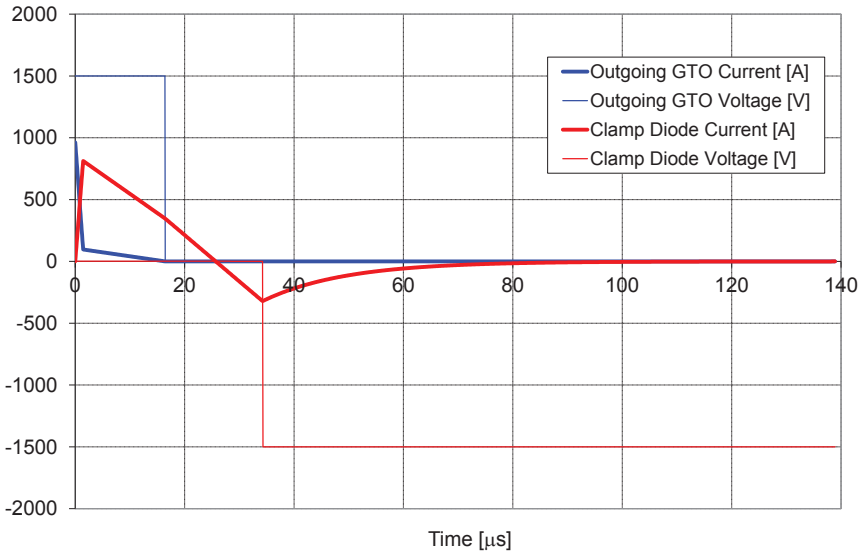


Fig. C.9 Simulated Device Power Dissipation for 24 Phase Commutator Devices

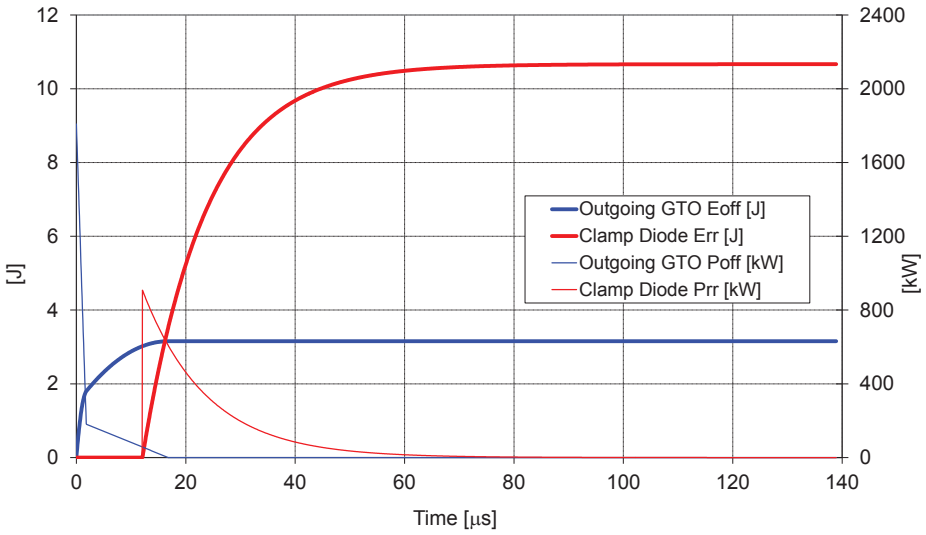
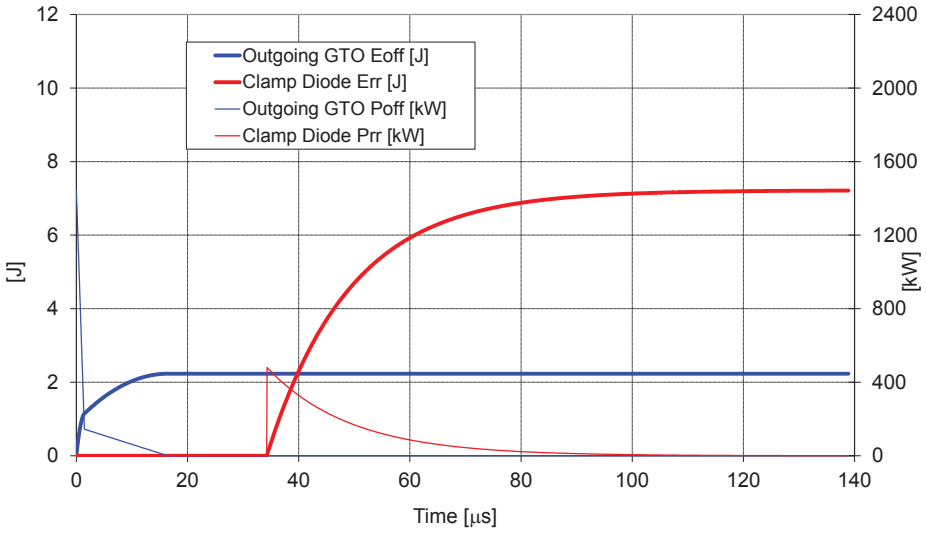


Fig. C.10 Simulated Device Power Dissipation for 15 Phase Commutator Devices



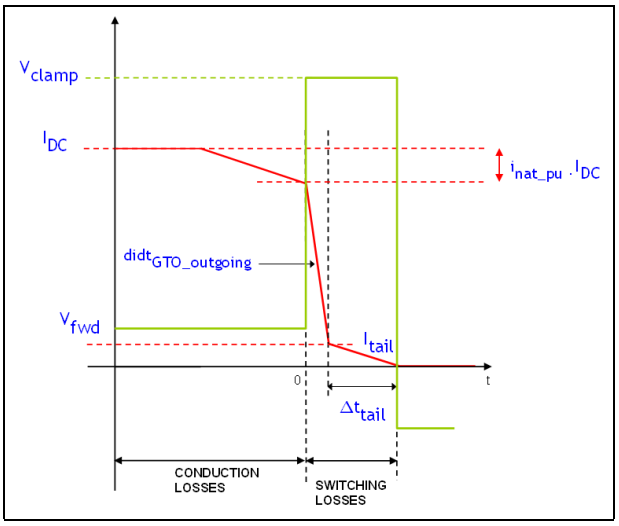
Appendix D

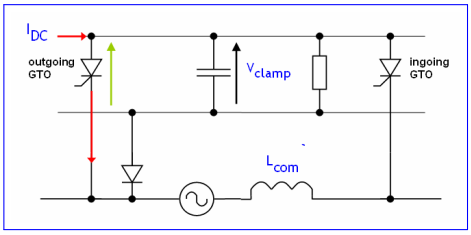
Mathcad Calculations: Phase Comparison

D.1 Mathcad Model for Power Dissipation

The aim of this spreadsheet is to estimate:
- the GTO conduction losses.
- the GTO turn-off switching losses.
- the clamp diode conduction losses.
- the clamp diode reverse recovery losses.

INPUT DATA





GTO Data
(Based on ABB GTO 5SGA 15F2502)

didt of the outgoing GTO [A/s]

$didt_{GTO\_outgoing} := \frac{-0.8 \cdot 1500}{2 \cdot 10^{-6}}$

Tail current duration [s]

$\Delta t_{tail} := 15 \cdot 10^{-6}$

Device forward voltage drop at 125 deg C [V]

$V_{fwd}(i) = A_{Tvj} + B_{Tvj} \cdot i + C_{Tvj} \cdot \ln(i + 1) + D_{Tvj} \cdot \sqrt{i}$

$A_{Tvj} := 11.7 \cdot 10^{-3}$

$B_{Tvj} := 630.8 \cdot 10^{-6}$

$C_{Tvj} := 340.2 \cdot 10^{-3}$

$D_{Tvj} := -22.0 \cdot 10^{-3}$

Clamp Diode Data
(Based on ABB Rectifier Diode 5SDD 08D5000)

Clamp diode forward voltage [V]

$V_{diode\_fwd}(i_{diode}) := 0.984 + 0.487 \cdot 10^{-3} \cdot i_{diode}$

Clamp diode reverse recovery charge [C]

$Q_{rr}(didt, i_{forced}) := (0.00095 \cdot \ln(didt) - 0.013) \cdot \frac{i_{forced}}{1000}$

Clamp diode peak reverse recovery current [A]

$I_{rr}(didt, i_{forced}) := -\left(-4 \cdot 10^{-14} \cdot didt^2 + 9 \cdot 10^{-6} \cdot didt + 52.379\right) \cdot \frac{i_{forced}}{1000}$

Electronic Commutator Data

Operating mean clamp voltage [V]

$V_{clamp} := 1500$

Operating DC link current [A]

24 phases: $I_{DC\_24} := 2411$

15 phases: $I_{DC\_15} := 1926$

Current which has been naturally commutated during the natural overlap angle [pu of operating DC link current]

$i_{nat\_pu} := 0.5$

Machine Data

Commutating inductance [H] (24 phase machine)

$L_{com} := 10 \cdot 10^{-6}$

$L_{24} := L_{com}$

$L_{15} := 4 \cdot L_{24}$

Operating electrical frequency [Hz]

$f_e := 10$

Rated power [W] (for efficiency calcs)

$P_n := 2 \cdot 10^6$

Misc

Number of points for calculations

$N_{points} := 2000$

INPUT DATA

CALCULATIONS

Misc Variable Definitions

Variable for phase number

$N_{24} := 24$

$N_{15} := 15$

Electrical period [s]

$T_e(f) := \frac{1}{f}$

Duty cycle i.e. electrical period divided by phase number [s]

$\tau_{duty}(n, f) := \frac{T_e(f)}{n}$

Graph Variables

Define graph variable ranges (time and current increments)

$t_{g2\_end} := \frac{\tau_{duty}(N_{24}, f_e)}{30}$

$t_{g2} := 0 \cdot s, \frac{t_{g2\_end}}{N_{points}} .. t_{g2\_end}$

$i_g := 0.05, 0.1 .. 1$

GTO Current & Voltage Waveforms

GTO tail current [A] (assume 10% of forced commutated current)

$I_{tail}(i_{forced}) := 0.1 \cdot i_{forced}$

Instant at which the current in the GTO starts to tail [s]

$t_{tail}(i_{dc}, i_{nat\_pu}) := \frac{I_{tail}(i_{dc} - i_{nat\_pu} \cdot i_{dc}) - (i_{dc} - i_{nat\_pu} \cdot i_{dc})}{didt_{GTO\_outgoing}}$

Note that:
$i_{dc} - i_{nat\_pu} \cdot i_{dc} = i_{forced}$

didt of the ingoing GTO [A/s]

$didt_{GTO\_ingoing}(v, l) := \frac{v}{l}$

Current in the ingoing GTO [A]

$$i_{GTO\_ingoing}(t, v, l, i_{dc}, i_{nat\_pu}) := \begin{cases} i_{nat\_pu} \cdot i_{dc} + didt_{GTO\_ingoing}(v, l) \cdot t & \text{if } i_{nat\_pu} \cdot i_{dc} + didt_{GTO\_ingoing}(v, l) \cdot t \le i_{dc} \\ i_{dc} & \text{otherwise} \end{cases}$$

Current in the outgoing GTO [A]

$$i_{GTO\_outgoing}(t, i_{dc}, i_{nat\_pu}) := \begin{cases} i_{dc} - i_{nat\_pu} \cdot i_{dc} + didt_{GTO\_outgoing} \cdot t & \text{if } t < t_{tail}(i_{dc}, i_{nat\_pu}) \\ \frac{-I_{tail}(i_{dc} - i_{nat\_pu} \cdot i_{dc})}{\Delta t_{tail}} \cdot t + I_{tail}(i_{dc} - i_{nat\_pu} \cdot i_{dc}) \cdot \left(1 + \frac{t_{tail}(i_{dc}, i_{nat\_pu})}{\Delta t_{tail}}\right) & \text{if } t_{tail}(i_{dc}, i_{nat\_pu}) \le t \le t_{tail}(i_{dc}, i_{nat\_pu}) + \Delta t_{tail} \\ 0 & \text{if } t \ge t_{tail}(i_{dc}, i_{nat\_pu}) + \Delta t_{tail} \end{cases}$$

Outgoing GTO voltage [V] (GTO assumed to turn-off into clamp voltage, then assumed to be zero once the current is zero for turn-off switching calculations)

$$v_{GTO\_outgoing}(t, i_{dc}, i_{nat\_pu}, v) := \begin{cases} v & \text{if } 0 \le t \le t_{tail}(i_{dc}, i_{nat\_pu}) + \Delta t_{tail} \\ 0 & \text{if } t > t_{tail}(i_{dc}, i_{nat\_pu}) + \Delta t_{tail} \end{cases}$$

Clamp Diode Current Waveforms

Time at which the clamp diode reached zero [s]

$$t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu}) := \frac{i_{dc} - i_{nat\_pu} \cdot i_{dc}}{didt_{GTO\_ingoing}(v, l)}$$

Time at which the clamp diode turns off [s]

$$t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) := t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu}) - I_{rr}\left(\frac{v}{l}, i_{dc} - i_{nat\_pu} \cdot i_{dc}\right) \cdot \frac{l}{v}$$

Clamp diode decay time constant [s] (formula based on ABB Application Note: Design of RC Snubbers for Phase Control Applications)

$$\tau = \frac{Q_{rr}}{I_{rr}} - \frac{I_{rr}}{2 \cdot di/dt}$$

$$\tau(v, l, i_{dc}, i_{nat\_pu}) := \frac{Q_{rr}\left(\frac{v}{l}, i_{dc} - i_{nat\_pu} \cdot i_{dc}\right)}{-I_{rr}\left(\frac{v}{l}, i_{dc} - i_{nat\_pu} \cdot i_{dc}\right)} - \frac{-I_{rr}\left(\frac{v}{l}, i_{dc} - i_{nat\_pu} \cdot i_{dc}\right)}{2 \cdot \frac{-v}{l}}$$

Clamp diode reverse recovery current [A]

$$i_{diode\_rr}(t, v, l, i_{dc}, i_{nat\_pu}) := I_{rr}\left(\frac{v}{l}, i_{dc} - i_{nat\_pu} \cdot i_{dc}\right) \cdot \exp\left(\frac{-t + t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu})}{\tau(v, l, i_{dc}, i_{nat\_pu})}\right)$$

Current in the clamp diode [A]

$$i_{diode}(t, v, l, i_{dc}, i_{nat\_pu}) := \begin{cases} i_{dc} - i_{GTO\_ingoing}(t, v, l, i_{dc}, i_{nat\_pu}) - i_{GTO\_outgoing}(t, i_{dc}, i_{nat\_pu}) & \text{if } 0 \le t \le t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu}) \\ \left[\frac{-v}{l} \cdot (t - t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu}))\right] & \text{if } t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu}) < t \le t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) \\ i_{diode\_rr}(t, v, l, i_{dc}, i_{nat\_pu}) & \text{if } (t > t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu})) \end{cases}$$

Clamp diode RMS Current [A]

$$I_{diode\_RMS}(v, l, i_{dc}, i_{nat\_pu}) := \sqrt{\frac{1}{T_e(f_e)} \cdot \int_0^{t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu})} \left(i_{diode}(t, v, l, i_{dc}, i_{nat\_pu})\right)^2 dt}$$

Clamp diode voltage [V]

$$v_{diode}(t, v, l, i_{dc}, i_{nat\_pu}) := \begin{cases} V_{diode\_fwd}(i_{diode}(t, v, l, i_{dc}, i_{nat\_pu})) & \text{if } 0 \le t \le t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) \\ -v \text{ if } t > t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) \end{cases}$$

GTO Losses

Outgoing GTO turn-off power [W]

$$P_{GTO\_off}(t, i_{dc}, i_{nat\_pu}, v) := v_{GTO\_outgoing}(t, i_{dc}, i_{nat\_pu}, v) \cdot i_{GTO\_outgoing}(t, i_{dc}, i_{nat\_pu})$$

Outgoing GTO turn-off energy [J]

$$E_{GTO\_off}(t, i_{dc}, i_{nat\_pu}, v) := \int_0^t P_{GTO\_off}(u, i_{dc}, i_{nat\_pu}, v)\, du$$

Outgoing GTO mean turn-off power [W]

$$P_{GTO\_off\_mean}(i_{dc}, i_{nat\_pu}, v, l) := f_e \cdot E_{GTO\_off}(t_{diode\_zero}(v, l, i_{dc}, i_{nat\_pu}), i_{dc}, i_{nat\_pu}, v)$$

$$P_{GTO\_off\_mean\_total}(i_{dc}, i_{nat\_pu}, v, l, n) := 2n \cdot P_{GTO\_off\_mean}(i_{dc}, i_{nat\_pu}, v, l)$$

GTO forward voltage drop [V]

$$V_{fwd}(i) := A_{Tvj} + B_{Tvj} \cdot i + C_{Tvj} \cdot \ln(i + 1) + D_{Tvj} \cdot \sqrt{i}$$

GTO conduction losses [W]

$$P_{GTO\_cond}(i_{dc}) := V_{fwd}(i_{dc}) \cdot i_{dc}$$

$$P_{GTO\_cond\_mean}(i_{dc}, n) := \frac{1}{n} \cdot P_{GTO\_cond}(i_{dc})$$

$$P_{GTO\_cond\_mean\_total}(i_{dc}, n) := 2 \cdot n\, P_{GTO\_cond\_mean}(i_{dc}, n)$$

Clamp Diode Losses

Clamp diode power losses [W]

$$p_{diode}(t, v, l, i_{dc}, i_{nat\_pu}) := v_{diode}(t, v, l, i_{dc}, i_{nat\_pu}) \cdot i_{diode}(t, v, l, i_{dc}, i_{nat\_pu})$$

Clamp diode power dissipation due to conduction losses [W]

$$E_{diode\_cond}(t, v, l, i_{dc}, i_{nat\_pu}) := \begin{cases} \int_0^t \left| p_{diode}(u, v, l, i_{dc}, i_{nat\_pu}) \right| du & \text{if } 0 \le t \le t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) \\ \int_0^{t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu})} \left| p_{diode}(u, v, l, i_{dc}, i_{nat\_pu}) \right| du & \text{otherwise} \end{cases}$$

$$P_{diode\_cond\_mean}(v, l, i_{dc}, i_{nat\_pu}) := f_e \cdot E_{diode\_cond}(t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}), v, l, i_{dc}, i_{nat\_pu})$$

$$P_{diode\_cond\_mean\_total}(v, l, i_{dc}, i_{nat\_pu}, n) := 2n \cdot P_{diode\_cond\_mean}(v, l, i_{dc}, i_{nat\_pu})$$

Clamp diode power dissipation due to reverse recovery losses [W]

$$E_{diode\_rr}(t, v, l, i_{dc}, i_{nat\_pu}) := \begin{cases} 0 & \text{if } 0 \le t < t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) \\ \int_{t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu})}^t p_{diode}(u, v, l, i_{dc}, i_{nat\_pu}) du & \text{if } t \ge t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) \end{cases}$$

$$P_{diode\_rr\_mean}(v, l, i_{dc}, i_{nat\_pu}) := f_e \cdot E_{diode\_rr}(t_{diode\_off}(v, l, i_{dc}, i_{nat\_pu}) + 10 \cdot \tau(v, l, i_{dc}, i_{nat\_pu}), v, l, i_{dc}, i_{nat\_pu})$$

After $10\,\tau$ reverse recovery current has reached zero.

$$P_{diode\_rr\_mean\_total}(v, l, i_{dc}, i_{nat\_pu}, n) := 2n \cdot P_{diode\_rr\_mean}(v, l, i_{dc}, i_{nat\_pu})$$

RESULTS

GTO Losses

Total electronic commutator GTO turn-off switching losses

$$P_{GTO\_off\_mean\_total}(I_{DC\_24}, i_{nat\_pu}, V_{clamp}, L_{24}, N_{24}) = 1.292 \times 10^3$$

$$P_{GTO\_off\_mean\_total}(I_{DC\_24}, i_{nat\_pu}, V_{clamp}, L_{15}, N_{15}) = 946.368$$

$$\frac{P_{GTO\_cond\_mean\_total}(I_{DC\_24}, N_{24})}{48}\,s = 311.608$$

$$P_{GTO\_cond\_mean\_total}(I_{DC\_15}, N_{15}) = 1.092 \times 10^4$$

Total Losses

Total electronic commutator losses due GTO turn-off losses & Clamp diode losses

$$P_{total\_mean}(V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu}, N_{24}) = 2.137 \times 10^4$$

$$P_{total\_mean}(V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu}, N_{15}) = 1.376 \times 10^4$$

Efficiency

$$\eta(V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu}, N_{24}) = 98.931$$

$$\eta(V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu}, N_{15}) = 99.312$$

Clamp Diode Losses

Total electronic commutator clamp diode conduction losses

$$P_{diode\_cond\_mean\_total}(V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu}, N_{24}) = 2.308$$

$$P_{diode\_cond\_mean\_total}(V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu}, N_{15}) = 4.45$$

Total electronic commutator clamp diode reverse recovery losses

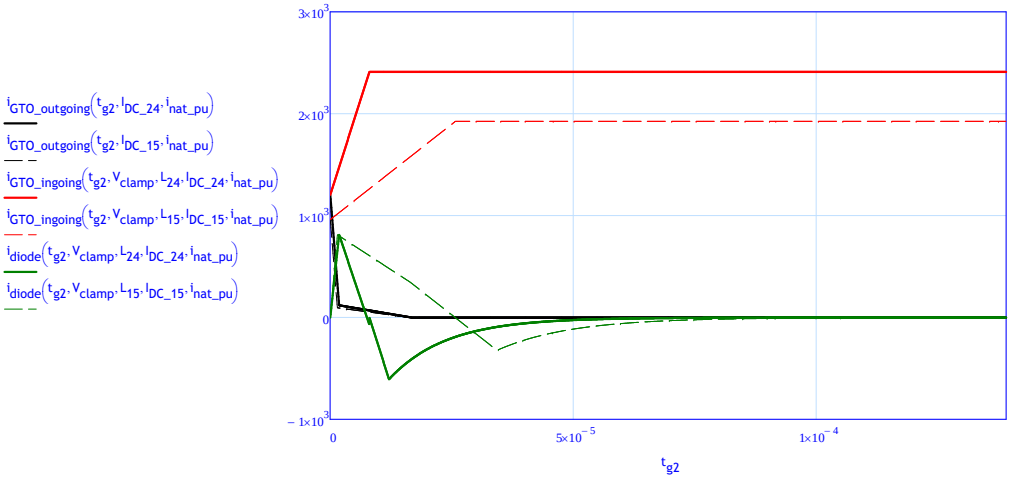
$$P_{diode\_rr\_mean\_total}(V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu}, N_{24}) = 5.12 \times 10^3$$

$$P_{diode\_rr\_mean\_total}(V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu}, N_{15}) = 2.165 \times 10^3$$

Clamp diode RMS current

$$I_{diode\_RMS}(V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu}) = 4.08$$

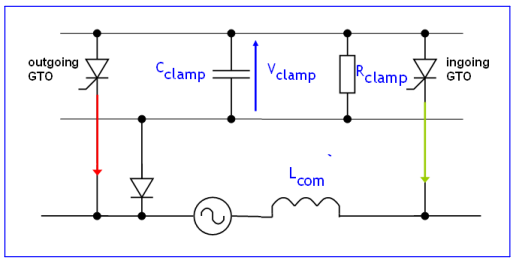
$$I_{diode\_RMS}(V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu}) = 7.743$$

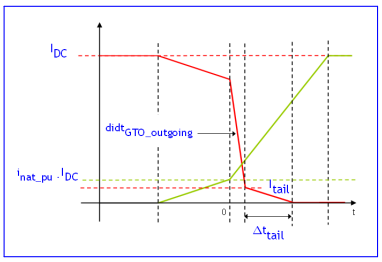

$i_{GTO\_outgoing}(t_{g2}, I_{DC\_24}, i_{nat\_pu})$
$i_{GTO\_outgoing}(t_{g2}, I_{DC\_15}, i_{nat\_pu})$
$i_{GTO\_ingoing}(t_{g2}, V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu})$
$i_{GTO\_ingoing}(t_{g2}, V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu})$
$i_{diode}(t_{g2}, V_{clamp}, L_{24}, I_{DC\_24}, i_{nat\_pu})$
$i_{diode}(t_{g2}, V_{clamp}, L_{15}, I_{DC\_15}, i_{nat\_pu})$
3×10^{3}
2×10^{3}
1×10^{3}
0
-1×10^{3}
0
5×10^{-5}
1×10^{-4}
t_{g2}

D.2 Mathcad Model for Clamp Rating

The aim of this spreadsheet is to determine the clamp voltage.

INPUT DATA





GTO Data

didt of the outgoing GTO [A/s]

$didt_{GTO\_outgoing} := \frac{-0.8 \cdot 1500}{2 \cdot 10^{-6}} \cdot \frac{A}{s}$

Tail current duration [s]

$\Delta t_{tail} := 1 \cdot 15 \cdot 10^{-6} \cdot s$

Electronic Commutator

Operating DC link current [A]

$I_{DC\_24} := 2411 \cdot A$

$I_{DC\_15} := 1926 \cdot A$

Current which has been naturally commutated during the natural overlap angle [pu of operating Idc]

$i_{nat\_pu} := 0.5$

Machine Data

Commutating inductance [H]

$L_{com} := 10 \cdot 10^{-6} \cdot H$

$L_{24} := L_{com}$

$L_{15} := 4 \cdot L_{24}$

Operating electrical frequency [Hz]

$f_e := 10 \cdot Hz$

Misc

Number of points for calculations

$N_{points} := 200$

Tolerance for clamp voltage calculations

$V_{tol} := 0.1 \cdot V$

Initial voltage for clamp voltage calculations

$V_{loop\_start} := 1000 \cdot V$

Clamp Components

Clamp capacitance [F]

$C_{clamp} := 100 \cdot 10^{-6} \cdot F$

$C_{clamp\_N24} := C_{clamp}$

$C_{clamp\_N15} := 1.5 C_{clamp\_N24}$

Clamp discharge resistance [Ω]

$R_{clamp} := 4 \cdot 500 \cdot \Omega$

$R_{clamp\_N24} := R_{clamp}$

$R_{clamp\_N15} := 0.445 R_{clamp\_N24}$

INPUT DATA

CALCULATIONS

Misc Variable Definition

Variable for phase number

$N_{24} := 24$

$N_{15} := 15$

Electrical period [s]

$T_e(f) := \frac{1}{f}$

Duty cycle i.e. electrical period divided by phase number [s]

$\tau_{duty}(n, f) := \frac{T_e(f)}{n}$

Integer indexing the number of duty cycles withing 1 electrical period

$N_\tau(t, n, f) := floor\left(\frac{t}{\tau_{duty}(n, f)}\right)$

Time constant of the RC discharge circuit [s]

$\tau_{clamp}(r, c) := r \cdot c$

Define graph time ranges

$t_{g1\_end} := \tau_{duty}(N_{15}, f_e)$

$t_{g2\_end} := \frac{\tau_{duty}(N_{24}, f_e)}{20}$

$t_{g1} := 0 \cdot s, \frac{t_{g1\_end}}{N_{points}} .. t_{g1\_end}$

$t_{g2} := 0 \cdot s, \frac{t_{g2\_end}}{N_{points}} .. t_{g2\_end}$

Define misc graph ranges

$i_{g\_pu} := 0.2, 0.4 .. 1$ Current increment

$r_{g\_pu} := 1, 1.2 .. 3$ Clamp discharge resistance increment

$c_{g\_pu} := 1, 1.2 .. 2$ Clamp capacitance increment

GTO Current Waveforms

GTO tail current [A] (assume 10% of the forced commutated current)

$$I_{tail}(i, i_{nat\_pu}) := 0.1 \cdot (i - i_{nat\_pu} \cdot i)$$

Instant at which the current in the GTO starts to tail [s]

$$t_{tail}(i, i_{nat\_pu}) := \frac{I_{tail}(i, i_{nat\_pu}) - (i - i_{nat\_pu} \cdot i)}{didt_{GTO\_outgoing}}$$

didt of the ingoing GTO [A/s]

$$didt_{GTO\_ingoing}(v, l) := \frac{v}{l}$$

Current in the ingoing GTO [A]

$$i_{GTO\_ingoing}(t, v, l, i, i_{nat\_pu}) := \begin{cases} i_{nat\_pu} \cdot i + didt_{GTO\_ingoing}(v, l) \cdot t & \text{if } i_{nat\_pu} \cdot i + didt_{GTO\_ingoing}(v, l) \cdot t \le i \\ i & \text{otherwise} \end{cases}$$

Current in the outgoing GTO [A]

$$i_{GTO\_outgoing}(t, i, i_{nat\_pu}) := \begin{cases} i - i_{nat\_pu} \cdot i + didt_{GTO\_outgoing} \cdot t & \text{if } t < t_{tail}(i, i_{nat\_pu}) \\ \frac{-I_{tail}(i, i_{nat\_pu})}{\Delta t_{tail}} \cdot t + I_{tail}(i, i_{nat\_pu}) \cdot \left(1 + \frac{t_{tail}(i, i_{nat\_pu})}{\Delta t_{tail}}\right) & \text{if } t_{tail}(i, i_{nat\_pu}) \le t \le t_{tail}(i, i_{nat\_pu}) + \Delta t_{tail} \\ 0 & \text{if } t \ge t_{tail}(i, i_{nat\_pu}) + \Delta t_{tail} \end{cases}$$

Clamp Diode Current Waveforms

Current in the clamp diode [A]

$$i_{diode}(t, v, l, i, i_{nat\_pu}) := \begin{cases} i - i_{GTO\_ingoing}(t, v, l, i, i_{nat\_pu}) - i_{GTO\_outgoing}(t, i, i_{nat\_pu}) \\ 0 \quad \text{if } \left(i - i_{GTO\_ingoing}(t, v, l, i, i_{nat\_pu}) - i_{GTO\_outgoing}(t, i, i_{nat\_pu})\right) < 0 \end{cases}$$

Time at which the clamp diode turns off (assuming no reverse recovery current) [s]

$$t_{diode\_off}(v, l, i, i_{nat\_pu}) := \frac{i - i_{nat\_pu} \cdot i}{didt_{GTO\_ingoing}(v, l)}$$

Commutating Coil Current Waveforms

Current in the commutating coil [A]

$$i_{coil}(t, v, l, i, i_{nat\_pu}) := \frac{i}{2} - i_{GTO\_ingoing}(t, v, l, i, i_{nat\_pu})$$

CLamp Capacitor Voltage Waveforms

Clamp capacitor voltage definition for determining steady-state values [V] (charge and discharge)

$$v_{clamp\_temp}(t, v, l, c, i, i_{nat\_pu}, r) := \begin{cases} v + \frac{1}{c} \cdot \int_0^t i_{diode}(u, v, l, i, i_{nat\_pu})\, du & \text{if } 0 \le t \le t_{diode\_off}(v, l, i, i_{nat\_pu}) \\ v_{clamp\_temp}(t_{diode\_off}(v, l, i, i_{nat\_pu}), v, l, c, i, i_{nat\_pu}, r) \cdot \exp\left[\frac{-(t - t_{diode\_off}(v, l, i, i_{nat\_pu}))}{\tau_{clamp}(r, c)}\right] & \text{if } t > t_{diode\_off}(v, l, i, i_{nat\_pu}) \end{cases}$$

Determine the initial clamp voltage in steady-state [V]

$$V_{clamp0}(l, c, i, i_{nat\_pu}, n, f, r) := \begin{cases} temp \leftarrow V_{loop\_start} \\ \text{while } \left| v_{clamp\_temp}(\tau_{duty}(n, f), temp, l, c, i, i_{nat\_pu}, r) - temp \right| > V_{tol} \\ \quad temp \leftarrow v_{clamp\_temp}(\tau_{duty}(n, f), temp, l, c, i, i_{nat\_pu}, r) \\ temp \end{cases}$$

$$V_{clamp\_counter}(l, c, i, i_{nat\_pu}, n, f, r) := \begin{cases} temp \leftarrow V_{loop\_start} \\ k \leftarrow 1 \\ \text{while } \left| v_{clamp\_temp}(\tau_{duty}(n, f), temp, l, c, i, i_{nat\_pu}, r) - temp \right| > V_{tol} \\ \quad \begin{cases} temp \leftarrow v_{clamp\_temp}(\tau_{duty}(n, f), temp, l, c, i, i_{nat\_pu}, r) \\ k \leftarrow k + 1 \end{cases} \\ k \end{cases}$$

Clamp capacitor voltage definition over the duty cycle (charge and discharge) [V]

$$v_{clamp}(t, l, c, i, i_{nat\_pu}, n, f, r) := \begin{cases} temp \leftarrow V_{clamp0}(l, c, i, i_{nat\_pu}, n, f, r) \\ temp + \frac{1}{c} \cdot \int_0^t i_{diode}(u, temp, l, i, i_{nat\_pu})\, du & \text{if } 0 \le t \le t_{diode\_off}(temp, l, i, i_{nat\_pu}) \\ v_{clamp}(t_{diode\_off}(temp, l, i, i_{nat\_pu}), l, c, i, i_{nat\_pu}, n, f, r) \cdot \exp\left[\frac{-(t - t_{diode\_off}(temp, l, i, i_{nat\_pu}))}{\tau_{clamp}(r, c)}\right] & \text{if } t > t_{diode\_off}(temp, l, i, i_{nat\_pu}) \end{cases}$$

Clamp capacitor voltage ripple [V]

$$\Delta V_{clamp}(l, c, i, i_{nat\_pu}, n, f, r) := v_{clamp}(t_{diode\_off}(V_{clamp0}(l, c, i, i_{nat\_pu}, n, f, r), l, i, i_{nat\_pu}), l, c, i, i_{nat\_pu}, n, f, r) - v_{clamp}(0, l, c, i, i_{nat\_pu}, n, f, r)$$

Mean capacitor clamp voltage [V]

$$V_{clamp\_mean}(l, c, i, i_{nat\_pu}, n, f, r) := \frac{1}{\tau_{duty}(n, f)} \cdot \int_0^{\tau_{duty}(n, f)} v_{clamp}(t, l, c, i, i_{nat\_pu}, n, f, r)\, dt$$

Clamp capacitor voltage definition over the duty cycle (charge and discharge) [V]

$$v_{clamp\_1period}(t, l, c, i, i_{nat\_pu}, n, f, r) := \begin{cases} v_{clamp}(t, l, c, i, i_{nat\_pu}, n, f, r) & \text{if } 0 \le t \le \tau_{duty}(n, f) \\ v_{clamp}(t - N_{\tau}(t, n, f) \cdot \tau_{duty}(n, f), l, c, i, i_{nat\_pu}, n, f, r) & \text{otherwise} \end{cases}$$

Misc Graph Equations

Clamp voltage just before turn-off commutation

$V_{clamp0\_N24} := v_{clamp0}(L_{24}, C_{clamp\_N24}, I_{DC\_24}, i_{nat\_pu}, N_{24}, f_e, R_{clamp\_N24})$

$V_{clamp0\_N15} := v_{clamp0}(L_{15}, C_{clamp\_N15}, I_{DC\_15}, i_{nat\_pu}, N_{15}, f_e, R_{clamp\_N15})$

Clamp voltage at the end of the discharge

$V_{clamp\_end\_N24} := v_{clamp}(\tau_{duty}(N_{24}, f_e), L_{24}, C_{clamp\_N24}, I_{DC\_24}, i_{nat\_pu}, N_{24}, f_e, R_{clamp\_N24})$

$V_{clamp\_end\_N15} := v_{clamp}(\tau_{duty}(N_{15}, f_e), L_{15}, C_{clamp\_N15}, I_{DC\_15}, i_{nat\_pu}, N_{15}, f_e, R_{clamp\_N15})$

How many iteration to reach steady state

$N_{counter\_N24} := v_{clamp\_counter}(L_{24}, C_{clamp\_N24}, I_{DC\_24}, i_{nat\_pu}, N_{24}, f_e, R_{clamp\_N24})$

$N_{counter\_N15} := v_{clamp\_counter}(L_{24}, C_{clamp\_N15}, I_{DC\_15}, i_{nat\_pu}, N_{15}, f_e, R_{clamp\_N15})$

Ingoing GTO current waveform

$i_{GTO\_ingoing\_N24}(t) := i_{GTO\_ingoing}(t, V_{clamp0\_N24}, L_{24}, I_{DC\_24}, i_{nat\_pu})$

$i_{GTO\_ingoing\_N15}(t) := i_{GTO\_ingoing}(t, V_{clamp0\_N15}, L_{15}, I_{DC\_15}, i_{nat\_pu})$

Outgoing GTO current waveform

$i_{GTO\_outgoing\_N24}(t) := i_{GTO\_outgoing}(t, I_{DC\_24}, i_{nat\_pu})$

$i_{GTO\_outgoing\_N15}(t) := i_{GTO\_outgoing}(t, I_{DC\_15}, i_{nat\_pu})$

Clamp diode current waveform

$i_{diode\_N24}(t) := i_{diode}(t, V_{clamp0\_N24}, L_{24}, I_{DC\_24}, i_{nat\_pu})$

$i_{diode\_N15}(t) := i_{diode}(t, V_{clamp0\_N15}, L_{15}, I_{DC\_15}, i_{nat\_pu})$

Clamp voltage waveform

$v_{clamp\_N24}(t) := v_{clamp\_1period}(t, L_{24}, C_{clamp\_N24}, I_{DC\_24}, i_{nat\_pu}, N_{24}, f_e, R_{clamp\_N24})$

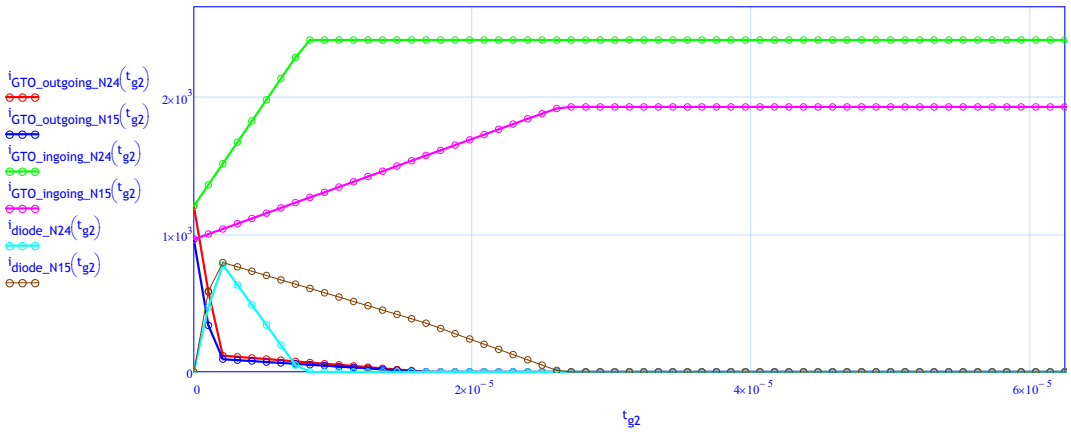
$v_{clamp\_N15}(t) := v_{clamp\_1period}(t, L_{15}, C_{clamp\_N15}, I_{DC\_15}, i_{nat\_pu}, N_{15}, f_e, R_{clamp\_N15})$

RESULTS

Misc Results & Checks

Min1 clamp voltage	Min2 clamp voltage (should be equal to Min1 Clamp Voltage)	Nb of iterations	Clamp voltage
$V_{clamp0\_N24} = 1481.2214852\,V$	$V_{clamp\_end\_N24} = 1481.316884\,V$	$N_{counter\_N24} = 106$	$\Delta V\_clamp\_N24 = 31.218331\,V$
$V_{clamp0\_N15} = 1462.0058976\,V$	$V_{clamp\_end\_N15} = 1462.1011246\,V$	$N_{counter\_N15} = 55$	$\Delta V\_clamp\_N15 = 74.6595071\,V$

Current Waveforms



D.3 Device Data Sheets

V_{RSM}	=	5200 V
I_{FAVM}	=	1028 A
I_{FRMS}	=	1614 A
I_{FSM}	=	12.8×10^3 A
V_{F0}	=	0.894 V
r_F	=	0.487 mΩ

Rectifier Diode
5SDD 08D5000

Doc. No. 5SYA1165-00 Jan. 03

- **Very low on-state losses**
- **Optimum power handling capability**

Blocking

Maximum rated values [1]

Parameter	Symbol	Conditions	Value	Unit
Repetetive peak reverse voltage	V_{RRM}	f = 50 Hz, t_p = 10ms, T_j = -40...160°C	5000	V
Non - repetetive peak reverse voltage	V_{RSM}	f = 5 Hz, t_p = 10ms, T_j = -40...160°C	5200	V

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. (reverse) leakage current	I_{RRM}	V_{RRM}, Tj = 160°C			30	mA

Mechanical data

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		8	10	12	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m			0.3		kg
Housing thickness	H			26		mm
Pole-piece diameter	D_P			34		mm
Surface creepage distance	D_S		30			mm
Air strike distance	D_a		18			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

On-state

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	I_{FAVM}	50 Hz, Half sine wave, T_C = 85 °C			1028	A
Max. RMS on-state current	I_{FRMS}				1614	A
Max. peak non-repetitive surge current	I_{FSM}	t_p = 10 ms, T_j = 160°C, V_R = 0 V			12.8×10^3	A
Limiting load integral	I^2t				682×10^3	A^2s
Max. peak non-repetitive surge current	I_{FSM}	t_p = 8.3 ms, T_j = 160°C, V_R = 0 V			12×10^3	A
Limiting load integral	I^2t				720×10^3	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_F	I_F = 1500 A, T_j = 160°C			1.65	V
Threshold voltage	$V_{(TO)}$	T_j = 160°C, I_T = 1500...4500 A			0.894	V
Slope resistance	r_T				0.487	mΩ

Switching

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_{rr}	di_F/dt = -30 A/µs, V_R = 100 V, I_{FRM} = 1000 A, T_j = 160°C		2400	3500	µAs

Thermal

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}		-40		160	°C
Storage temperature range	T_{stg}		-40		160	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled			32	K/kW
	$R_{th(j-c)A}$	Anode-side cooled			50	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled			88	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled			8	K/kW
	$R_{th(c-h)}$	Single-side cooled			16	K/kW

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	11.600	10.110	7.870	2.410
τ_i(s)	0.7033	0.2185	0.0588	0.0042

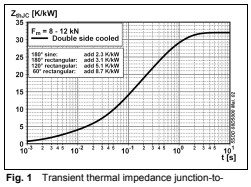


Fig. 1 Transient thermal impedance junction-to-case.

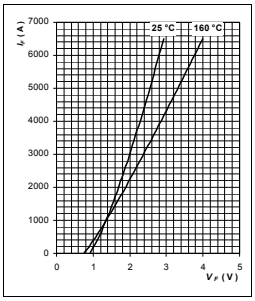


Fig. 2 Max. on-state characteristics.

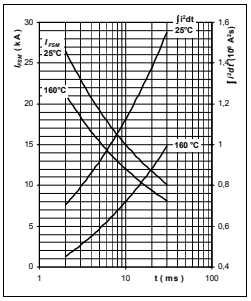


Fig. 3 Surge forward current vs. pulse length. Half sine wave, single pulse, V_R = 0 V

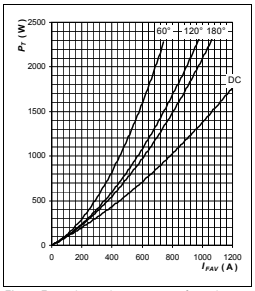


Fig. 4 Forward power loss vs. average forward current, sine waveform, f = 50 Hz

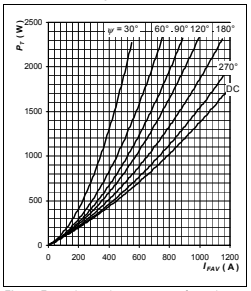


Fig. 5 Forward power loss vs. average forward current, square waveform, f = 50 Hz

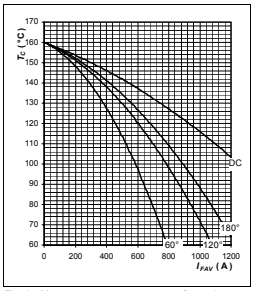


Fig. 6 Max. case temperature vs aver. forward current, sine waveform, f = 50 Hz

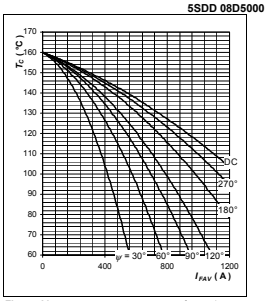


Fig. 7 Max. case temperature vs aver. forward current, square waveform, f = 50 Hz

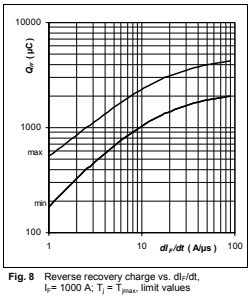


Fig. 8 Reverse recovery charge vs. di_F/dt, I_F= 1000 A; $T_j = T_{jmax}$, limit values

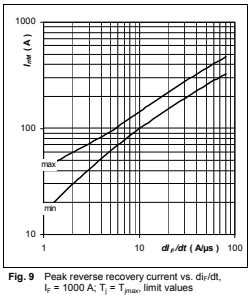


Fig. 9 Peak reverse recovery current vs. di_F/dt, I_F = 1000 A; $T_j = T_{jmax}$, limit values

V_{DRM}	=	2500 V
I_{TGQM}	=	1500 A
I_{TSM}	=	10×10³ A
V_{T0}	=	1.45 V
r_T	=	0.90 mW
V_{Dclink}	=	1400 V

Asymmetric Gate turn-off Thyristor
5SGA 15F2502

Doc. No. 5SYA1214-02 Oct. 06

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Annular gate electrode**
- **Industry standard housing**
- **Cosmic radiation withstand rating**

Blocking

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Repetitive peak off-state voltage	V_{DRM}	$V_{GR} \geq 2$ V			2500	V
Repetitive peak reverse voltage	V_{RRM}				17	V
Permanent DC voltage for 100 FIT failure rate	$V_{DC\text{-}link}$	Ambient cosmic radiation at sea level in open air.			1400	V

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Repetitive peak off-state current	I_{DRM}	$V_D = V_{DRM}$, $V_{GR} \geq 2$ V			100	mA
Repetitive peak reverse current	I_{RRM}	$V_R = V_{RRM}$, $R_{GK} = \infty$ Ω			50	mA

Mechanical data

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_m		14	15	16	kN

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Pole-piece diameter	D_p	± 0.1 mm		47		mm
Housing thickness	H		25.8		26.2	mm
Weight	m				0.6	kg
Surface creepage distance	D_s	Anode to Gate	25			mm
Air strike distance	D_a	Anode to Gate	15			mm

Note 1 Maximum rated values indicate limits beyond which damage to the device may occur

Gate

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Repetitive peak reverse voltage	V_{GRM}				17	V
Repetitive peak reverse current	I_{GRM}	$V_{GR} = V_{GRM}$			20	mA

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate trigger voltage	V_{GT}	T_{vj} = 25°C,		1.5		V
Gate trigger current	I_{GT}	V_D = 24 V, R_A = 0.1 Ω		1.5		A

Thermal

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Junction operating temperature	T_{vj}		0		125	°C
Storage temperature range	T_{stg}		0		125	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j\text{-}c)}$	Double side cooled			27	K/kW
	$R_{th(j\text{-}c)A}$	Anode side cooled			49	K/kW
	$R_{th(j\text{-}c)C}$	Cathode side cooled			60	K/kW
Thermal resistance case to heatsink (Double side cooled)	$R_{th(c\text{-}h)}$	Single side cooled			16	K/kW
	$R_{th(c\text{-}h)}$	Double side cooled			8	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	14.570	5.051	7.285	0.097
τ_i(s)	0.4610	0.0950	0.0120	0.0010

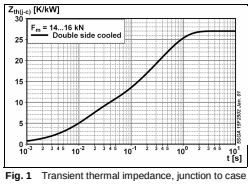


Fig. 1 Transient thermal impedance, junction to case

GTO Data

On-state

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	$I_{T(AV)M}$	Half sine wave, T_C = 85 °C			570	A
Max. RMS on-state current	$I_{T(RMS)}$				900	A
Max. peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125°C, sine wave After Surge: $V_D = V_R$ = 0 V			10×10^3	A
Limiting load integral	I^2t				500×10^3	A^2s
Max. peak non-repetitive surge current	I_{TSM}	t_p = 1 ms, T_{vj} = 125°C, sine wave After Surge: $V_D = V_R$ = 0 V			20×10^3	A
Limiting load integral	I^2t				200×10^3	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 1500 A, T_{vj} = 125°C			2.8	V
Threshold voltage	$V_{(T0)}$	T_{vj} = 125°C I_T = 300...2000 A			1.45	V
Slope resistance	r_T				0.90	mΩ
Holding current	I_H	T_{vj} = 25°C			50	A

Turn-on switching

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	di_T/dt_{cr}	T_{vj} = 125°C, I_T = 1500 A, I_{GM} = 30 A, di_G/dt = 20 A/µs f = 200 Hz			400	A/µs
Critical rate of rise of on-state current	di_T/dt_{cr}	f = 1 Hz			600	A/µs
Min. on-time	t_{on}	V_D = 0.5 V_{DRM}, T_{vj} = 125 °C I_T = 1500 A, di/dt = 100 A/µs, I_{GM} = 30 A, di_G/dt = 20 A/µs, C_S = 3 µF, R_S = 5 Ω	80			µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Turn-on delay time	t_d	V_D = 0.5 V_{DRM}, T_{vj} = 125 °C I_T = 1500 A, di/dt = 100 A/µs, I_{GM} = 30 A, di_G/dt = 20 A/µs, C_S = 3 µF, R_S = 5 Ω			2	µs
Rise time	t_r				4	µs
Turn-on energy per pulse	E_{on}				0.5	J

Turn-off switching

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. controllable turn-off current	I_{TGQM}	$V_{DM} \leq V_{DRM}$, di_{GQ}/dt = 30 A/µs, C_S = 3 µF, $L_S \leq 0.3$ µH			1500	A
Min. off-time	t_{off}	V_D = 0.5 V_{DRM}, T_{vj} = 125 °C $V_{DM} \leq V_{DRM}$, di_{GQ}/dt = 30 A/µs, $I_{TGQ} = I_{TGQM}$, R_S = 5 Ω, C_S = 3 µF, L_S = 0.3 µH	80			µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Storage time	t_s	V_D = 0.5 V_{DRM}, T_{vj} = 125 °C $V_{DM} \leq V_{DRM}$, di_{GQ}/dt = 30 A/µs, $I_{TGQ} = I_{TGQM}$, R_S = 5 Ω, C_S = 3 µF, L_S = 0.3 µH			15	µs
Fall time	t_f				2	µs
Turn-on energy per pulse	E_{off}				2	J
Peak turn-off gate current	I_{GQM}				480	A

Max. on-state characteristic model:

$$V_{T25} = A_{vj} + B_{vj} \cdot I_T + C_{vj} \cdot \ln(I_T + 1) + D_{vj} \cdot \sqrt{I_T}$$

Valid for I_T = 300 – 2000 A

A_{25}	B_{25}	C_{25}	D_{25}
178.9×10^{-3}	816.7×10^{-6}	356.4×10^{-3}	-41.7×10^{-3}

Max. on-state characteristic model:

$$V_{T125} = A_{vj} + B_{vj} \cdot I_T + C_{vj} \cdot \ln(I_T + 1) + D_{vj} \cdot \sqrt{I_T}$$

Valid for I_T = 300 – 2000 A

A_{125}	B_{125}	C_{125}	D_{125}
11.7×10^{-3}	630.8×10^{-6}	340.2×10^{-3}	-22.0×10^{-3}

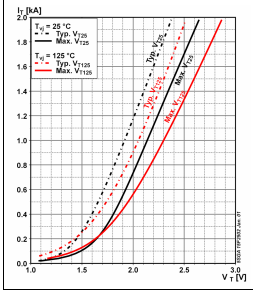


Fig. 2 On-state characteristics

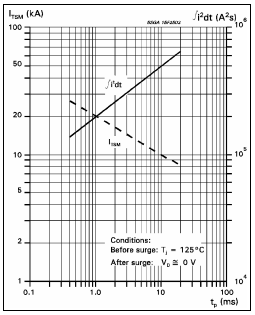


Fig. 3 Surge current and fusing integral vs. pulse width

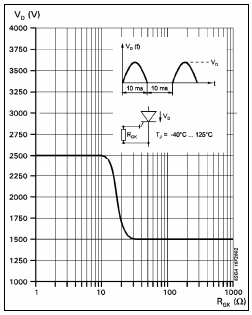


Fig. 4 Forward blocking voltage vs. gate-cathode resistance

5SGA 15F2502

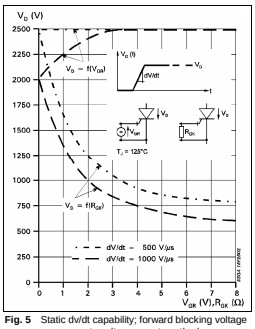


Fig. 5 Static dv/dt capability; forward blocking voltage vs. neg. gate voltage or gate cathode resistance

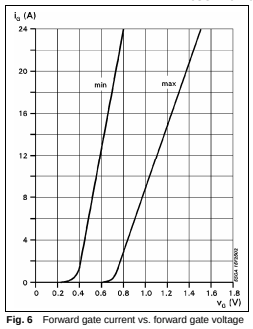


Fig. 6 Forward gate current vs. forward gate voltage

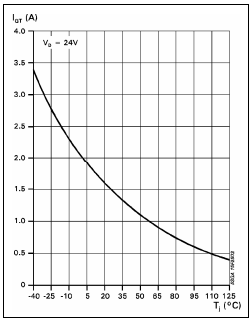


Fig. 7 Gate trigger current vs. junction temperature

5SGA 15F2502

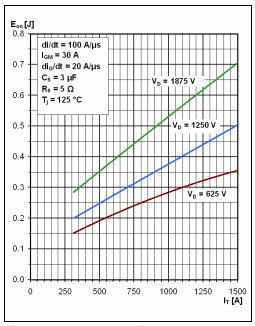


Fig. 8 Turn-on energy per pulse vs. on-state current and turn-on voltage

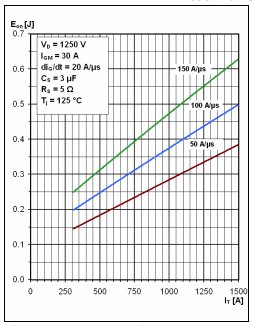


Fig. 9 Turn-on energy per pulse vs. on-state current and current rise rate

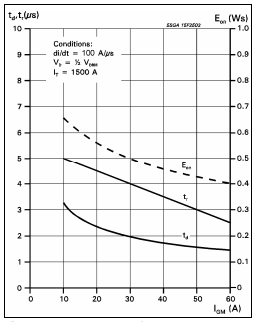


Fig. 10 Turn-on energy per pulse vs. on-state current and turn-on voltage

Common Test conditions:

di_G/dt	= 20 A/µs
C_S	= 3 µF
R_S	= 5 Ω
Tj	= 125 °C

Definition of Turn-on energy:

$$E_{on} = \int_0^{20\mu s} V_D \cdot I_T dt \quad (t = 0, I_G = 0.1 \cdot I_{GM})$$

Definition of Turn-off energy:

$$E_{off} = \int_0^{40\mu s} V_D \cdot I_T dt \quad (t = 0, I_T = 0.9 \cdot I_{TGQ})$$

5SGA 15F2502

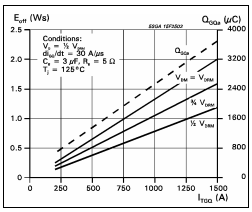


Fig. 11 Turn-off energy per pulse vs. turn-off current and peak turn-off voltage, extracted gate charge vs. turn-off current

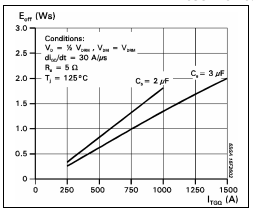


Fig. 12 Turn-off energy per pulse vs. turn-off current and snubber capacitance

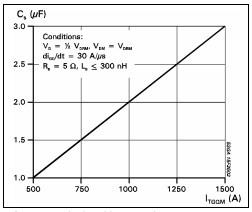


Fig. 13 Required snubber capacitor vs. max allowable turn-off current

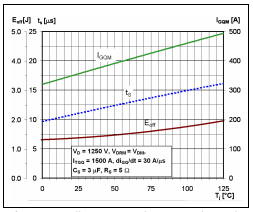


Fig. 14 Turn-off energy per pulse, storage time and peak turn-off gate current vs. junction temperature

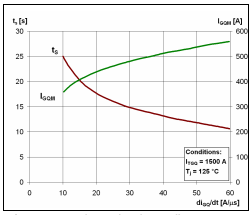


Fig. 15 Storage time and peak turn-off gate current vs. neg. gate current rise rate

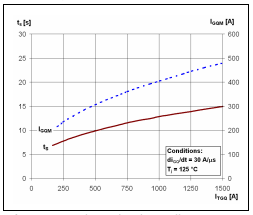


Fig. 16 Storage time and peak turn-off gate current vs. neg. gate current rise rate